

LOW POWER HIGHLY PROGRAMMABLE ANALOG FRONT-END FOR  
12-CHANNEL FULLY IMPLANTABLE COCHLEAR IMPLANTS

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ABDURRAHMAN BERKAY ÖZBEK

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12-CHANNEL FULLY IMPLANTABLE COCHLEAR IMPLANTS**

submitted by **ABDURRAHMAN BERKAY ÖZBEK** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering, Middle East Technical University** by,

Prof. Dr. Halil Kalıpçılar  
Dean, Graduate School of **Natural and Applied Sciences**

\_\_\_\_\_

Prof. Dr. İlkay Ulusoy  
Head of the Department, **Electrical and Electronics Eng.**

\_\_\_\_\_

Prof. Dr. Haluk Külâh  
Supervisor, **Electrical and Electronics Eng., METU**

\_\_\_\_\_

**Examining Committee Members:**

Prof. Dr. Tayfun Akın  
Electrical and Electronics Eng, METU

\_\_\_\_\_

Prof. Dr. Haluk Külâh  
Electrical and Electronics Eng, METU

\_\_\_\_\_

Prof. Dr. Ali Muhtaroglu  
Electrical and Electronics Eng, METU NCC

\_\_\_\_\_

Assoc. Prof. Dr. Serdar Kocaman  
Electrical and Electronics Eng, METU

\_\_\_\_\_

Assoc. Prof. Dr. Dinçer Gökçen  
Electrical and Electronics Eng, Hacettepe University

\_\_\_\_\_

Date: 17.12.2021

**I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.**

Name Last name : A. Berkay Özbek

Signature :

## ABSTRACT

### **LOW POWER HIGHLY PROGRAMMABLE ANALOG FRONT-END FOR 12-CHANNEL FULLY IMPLANTABLE COCHLEAR IMPLANTS**

Özbek, Abdurrahman Berkay  
Master of Science, Electrical and Electronics Engineering  
Supervisor : Prof. Dr. Haluk Külah

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Cochlear implants are the most common treatment option for individuals with sensorineural hearing loss. However, despite the functional success, the patients have concerns about the aesthetics and practicality of the device. Fully implantable cochlear implants (FICI), on the other hand, have a promising future to overcome these drawbacks by replacing the external components with an acoustic sensor and interface electronics. To achieve a high quality of hearing, the interface electronics should effectively decompose sound waves captured by the acoustic sensor into the frequency components while providing controllability of system parameters for personalized treatment and achieving low power consumption for the extension of battery life. In this thesis, a low-power low-noise highly-programmable analog front-end circuit has been designed to interface with the acoustic sensor of a 12-channel FICI.

First, a low-power highly-tunable biquadratic Gm-C bandpass filter has been designed and implemented as a part of the analog front-end. The center frequency and quality factor of the filter can be programmed between 200-6000 Hz and 1-3, respectively while consuming only 13.2 nW at 950 Hz. The filter achieved one of the best figure-of-merit compared to the analog bandpass filters in the literature.

Next, a complete analog front-end circuit to interface with the acoustic sensor of a 12-channel FICI system has been designed. The system can cover 85-6500 Hz and filter sound by 12 channels while providing channel-specific programmability for better speech perception and consuming only 9.03  $\mu$ W which is about 1.3% of the overall power consumption of the 12-channel FICI circuit.

Keywords: Fully Implantable Cochlear Implant, Analog Front-End, Auditory Signal Processing, Low-Power Biomedical Integrated Circuits

## ÖZ

### TAMAMEN İMPLANTE EDİLEBİLEN 12 KANALLI KOKLEAR İMPLANTLAR İÇİN YÜKSEK PROGRAMLANABİLİRLİK VE DÜŞÜK GÜÇ TÜKETİMLİ ANALOG ÖN-UÇ DEVRESİ

Özbek, Abdurrahman Berkay  
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği  
Tez Yöneticisi: Prof. Dr. Haluk Külâh

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Koklear implantlar, sensörinöral işitme kaybı olan bireyler için en yaygın tedavi seçeneğidir. Ancak koklear implantların fonksiyonel başarısına rağmen, hastalar cihazın estetiği ve pratikliği konusunda endişe duymaktadır. Öte yandan, tamamen implante edilebilir koklear implant sistemleri bir akustik sensör ve arayüz entegre devresi kullanarak implantın dış bileşenlerini ortadan kaldırıp bu dezavantajların üstesinden gelmek için umut verici bir geleceğe sahiptir. Yüksek kaliteli bir işitme elde etmek için, arayüz entegre devresi akustik sensör tarafından yakalanan ses dalgalarını frekans bileşenlerine etkili bir şekilde ayrıştırmalı, kişiselleştirilmiş tedavi adına sistem parametreleri için programlanabilirlik ve pil ömrünün uzatılması için düşük güç tüketimi sağlamalıdır. Bu tezde, 12 kanallı tamamen implante edilebilir bir koklear implant sisteminin akustik sensörüyle arayüz oluşturmak için düşük güçlü, düşük gürültülü, yüksek düzeyde programlanabilir bir analog ön uç devresi tasarlanmıştır.

İlk olarak, analog ön uç devresinin bir parçası olarak düşük güçlü, yüksek düzeyde programlanabilir ikinci derece  $G_m$ -C bant geçiren filtre tasarlanmış ve uygulanmıştır. Filtrenin merkez frekansı 200-6000 Hz aralığında ve filtrenin kalite faktörü 1-3

aralığında programlanabilmektedir. Filtre 950 Hz rezonans frekansında sadece 13,2 nW tüketmektedir ve literatürdeki analog bant geçiren filtrelerle kıyaslandığında en iyi performans metriklerinden birine ulaşmaktadır. Ardından, 12 kanallı tamamen implante edilebilir bir koklear implant sisteminin akustik sensörü ile arayüz oluşturmak için tüm bir arayüz elektroniği tasarlanmıştır. Tasarlanan analog ön uç devresi 85-6500 Hz aralığını kapsayabilmekte ve sesi 12 kanal ile filtreleyebilmektedir. Daha iyi işitme algısı için kanala özel programlanabilirlik sağlamak ve sadece 9,03  $\mu$ W güç tüketmektedir. Bu değer, 12 kanallı tamamen implante edilebilir koklear implant sisteminin toplam güç tüketiminin yaklaşık 1.3%'ü kadardır.

Anahtar Kelimeler: Tamamen İmplant Edilebilir Koklear İmplant, Analog Ön Uç, İşitsel Sinyal İşleme, Düşük Güç Tüketimli Biyomedikal Entegre Devreler

*To My Family Sema & Güzay Özbek*

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# CHAPTER 1

## INTRODUCTION

### 1.1 Motivation

World Health Organization (WHO) reports that 20% of the global population, which is almost 1.5 billion people, suffer from hearing losses. Depending on the degree of hearing loss, the disability is categorized as mild, moderate, severe, and profound. 1.16 billion people live with mild hearing loss while 400 million people live with moderate to severe hearing loss. Conventional hearing aids which simply amplify the acoustic sound can be utilized to deal with mild-to-severe hearing loss, However, for the rest which nearly 60 million people suffer from, cochlear implants which directly stimulate the auditory nerve would provide an effective treatment option [1]. It is reported that cochlear implants improve the speech perception of the patients and the majority of the cochlear implant users prefer to utilize the device in their daily life [2]. However, although cochlear implants have a high success rate in restoring hearing, the cochlear implant users might complain about the aesthetics and practicality of the device since the external components of the implant prevent the patients from using the device in some environments and attract people's attention. Dealing with these drawbacks is the main motivation behind the studies on fully implantable cochlear implants (FICI).

The sound processor should be miniaturized and the microphone should be replaced by an implantable acoustic sensor for a fully implantable cochlear implant system. There are several different approaches reported in the literature to sense the sound without a microphone, for example using a displacement sensor with piezoresistive electrodes [3], an intracochlear pressure sensor [4], a MEMS capacitive

accelerometer [5], and a piezoelectric sensor [6]. FLAMENCO project (A Fully-Implantable MEMS-Based Autonomous Cochlear Implant, [www.flamenco.metu.edu.tr](http://www.flamenco.metu.edu.tr)) is one of the promising fully implantable cochlear systems that replaces the microphone with a multi-channel piezoelectric acoustic transducer [7]. The transducer consists of eight cantilevers each of which resonates at a different frequency within the acoustic band so that it mechanically filters the sound. However, this transducer has several bottlenecks in terms of implantability and performance.

Firstly, the size ( $5 \times 5 \times 0.6$  mm) of the transducer is not compatible with the confined space of the middle ear as Figure 1.1 shows. Designing a multilayer structure would be a solution to this problem, but the cantilever length cannot be reduced for a target resonance at 300 Hz. Therefore, the implantation of the transducer onto the ossicles is almost impossible.

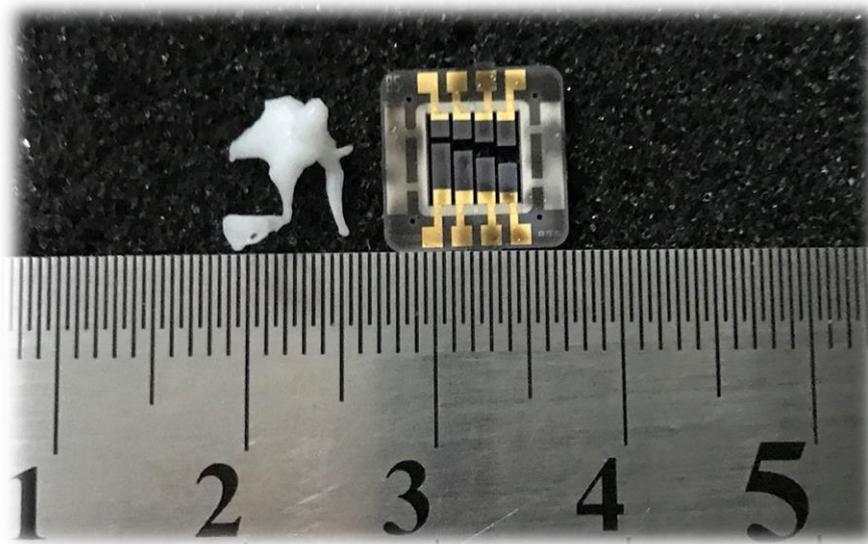


Figure 1.1. The size comparison of the ossicles and acoustic transducer.

Secondly, the cochlea filters each frequency in the hearing band continuously. However, cochlear implants filter specific frequencies discretely due to limited channel numbers. Therefore, the bandwidths of the channels should coincide with each other to some extent in order to cover the frequencies in between the channels as Figure 1.2 depicts [8]. However, due to the nature of the mechanical filtering, the

cantilevers of the transducer have very high quality factor ( $Q$ ) and narrow bandwidths, differing significantly from the ideal auditory filters, as Figure 1.3 indicates. Therefore, there are lost frequency bands in the frequency response of the transducer which results in significant degradation of speech perception.

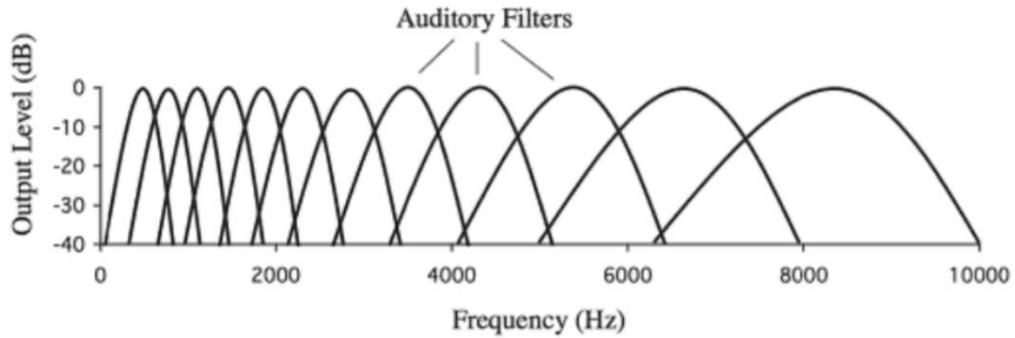


Figure 1.2. The frequency response of the auditory filters [8].

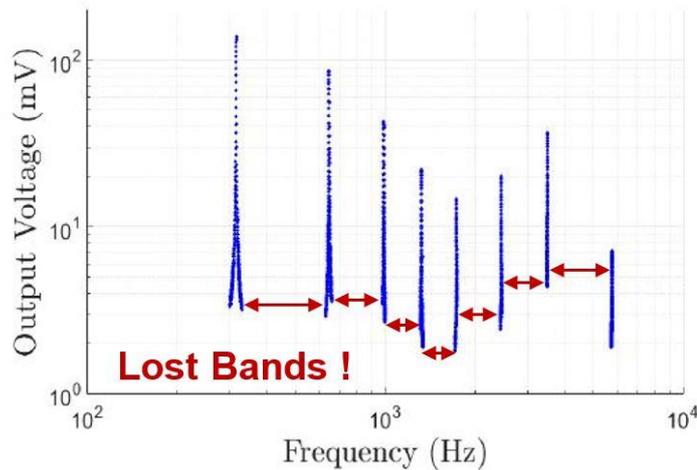


Figure 1.3. The frequency response of the multichannel acoustic transducer [7].

Lastly, the impedances of the cochlear electrodes may increase over time due to the build-up of fibrous tissue in the cochlea [9]. The increase in the impedance of the electrode would result in a failure in the operation of the related channel [10]. In addition, several electrodes of the implant might not be successfully implanted in the cochlear due to abnormalities such as cochlear otosclerosis and temporal bone fracture [11]. In such cases, the center frequencies and bandwidths of the remaining channels should be reconfigured such that the lost bands due to faulty channels are recovered. However, It is not possible to reconfigure the center frequencies and

bandwidths of the transducer channels after the fabrication since these are mechanically set before the fabrication.

To overcome these bottlenecks, an alternative system is proposed in the scope of the FLAMENCO project. Instead of the multichannel transducer, the new system utilizes a single-channel transducer as shown in Figure 1.4 (a) that has a resonance frequency far from the acoustic band and operates in the non-resonance region as summarized in Figure 1.4 (b). Thus, as there is a single-channel with a smaller channel length due to higher resonance frequency, it is possible to achieve a transducer with a smaller size which would be suitable for the confined space of the middle ear. Instead of mechanical filtering, the output of the single-channel acoustic transducer is processed by an analog front-end circuit so that the system would be able to provide programmable center frequencies and bandwidths.

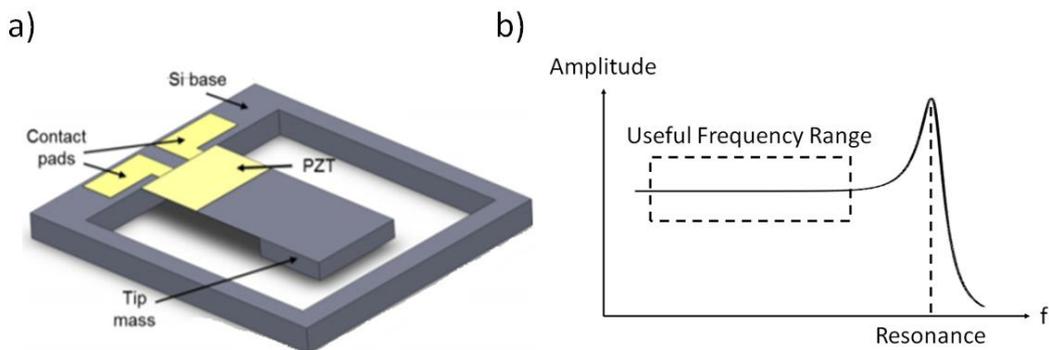


Figure 1.4. (a) The single-channel transducer [12], (b) the operation region of the single-channel transducer.

This thesis aims to design a low-power, low noise, and highly programmable analog front-end circuit for 12-channel fully implantable cochlear implants. The system is able to process a low-amplitude AC voltage generated by single-channel piezoelectric transducer operating in a non-resonance region, and filter the generated signal while providing the implant with programmability on the center frequency, bandwidth, and signal amplitude. The system consists of low noise amplifier (LNA), bandpass filterbank (BPFs) and variable gain amplifiers (VGA) as presented in Figure 1.5 which will be explained in the following chapters.

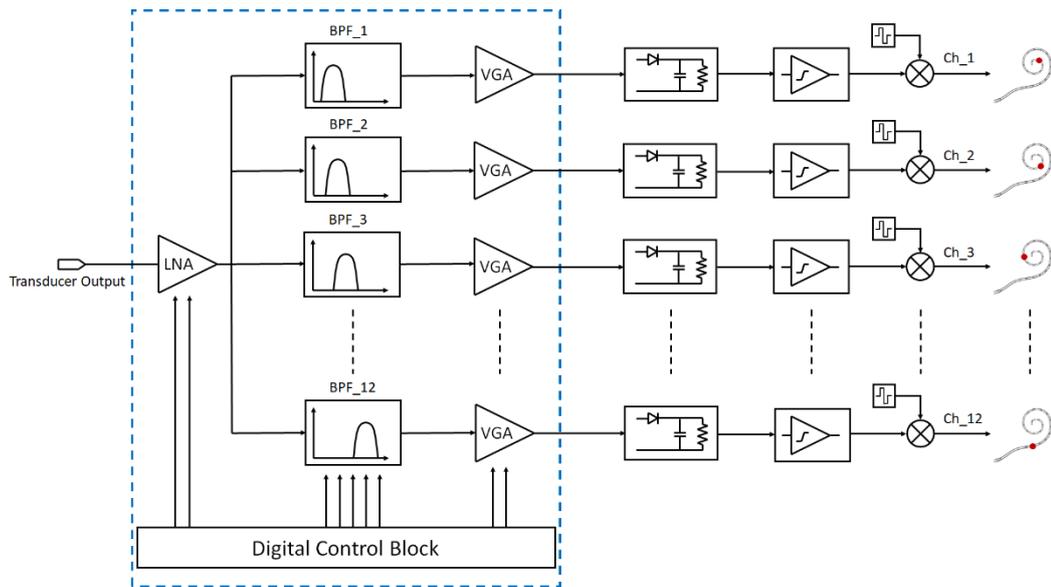


Figure 1.5. The proposed analog-front end circuit and interface electronics of the fully implantable cochlear implant system.

## 1.2 Hearing Mechanism

The ear is made up of three parts, namely the outer, middle, and inner ear as shown in Figure 1.6. The sound waves are collected by the pinna and transmitted to the tympanic membrane (eardrum) through the ear canal. The pressure of sound waves makes the tympanic membrane vibrate. This vibration is conducted from the eardrum to the oval window by the ossicles, the malleus, incus, and stapes. As the surface area of the tympanic membrane is larger than the surface area of the oval window and the length of the malleus is longer than the length of the incus, the sound is amplified while passing through the ossicles like a lever and hydraulic amplification. The vibration of the oval window triggers the movement of the cochlear fluid. As the fluid moves inside the cochlea, the thousands of nerve endings (hair cells) throughout the cochlea are put into motion. The stiffness and length of the nerve endings vary from base to apex of the cochlea so that each nerve ending has a different resonance frequency. The hair cells convert the mechanical vibration to the electrical signals and nerve impulses travel along the auditory nerve. These neural signals arrive at the auditory cortex of the brain and are interpreted as sound.



Figure 1.6. Anatomy of the ear [13].

### 1.3 Types and Treatments of Hearing Loss

Hearing loss can be defined as the partial or complete inability to hear sound in one or both ears and is caused by many factors such as aging, noise exposure, and genetics. Depending on the type of hearing loss, it is classified as conductive, sensorineural, and mixed hearing loss. The conductive hearing loss occurs when there is a problem with the transmission of the sound energy to the cochlea. One of the most common treatments for conductive hearing loss is hearing aids and amplifiers. These devices simply amplify the incoming sound and deliver the amplified sound into the ear canal to recover the loss. Other than hearing aids, the hearing amplifiers would only amplify the sound at the frequencies which the person struggles to hear. Sensorineural hearing loss, on the other hand, occurs when the hair cells in the cochlea are damaged or lost. Unlike conductive hearing loss, the sound energy is able to reach the cochlea without a loss in the sensorineural hearing loss. However, the damaged hair cells are not able to convert mechanical vibration to the electrical signals that stimulate the auditory nerve. Cochlear implant is the successful neural prosthesis for the treatment of sensorineural hearing loss since the damaged hair cells are bypassed and the auditory nerve is stimulated by the externally

generated electrical impulses. Mixed hearing loss is a combination of conductive and sensorineural problems. The hearing aids and the cochlear implants could be utilized together for the treatment of mixed hearing loss.

#### 1.4 Conventional Cochlear Implants

Cochlear implants are neural prostheses that electrically stimulate the auditory nerve and partially restore hearing. A cochlear implant has external and internal units as illustrated in Figure 1.7 (a). The external unit is placed behind the ear and consists of a microphone, speech processor, and RF transmitter. The microphone picks up the sound and converts it to electrical signals. The speech processor processes these signals and generates digital equivalent. The digital signal is transmitted to the internal unit through the RF link. The internal unit consists of a receiver/stimulator and electrode array. The receiver/stimulator decodes the transmitted signal and generates stimulation currents. The current pulses are sent to the electrode array inside the cochlea through wires and the auditory nerve is stimulated. The electrical impulses are transferred to the brain and interpreted as sound. Figure 1.7 (b) summarizes the operation of the modern cochlear implants [14].

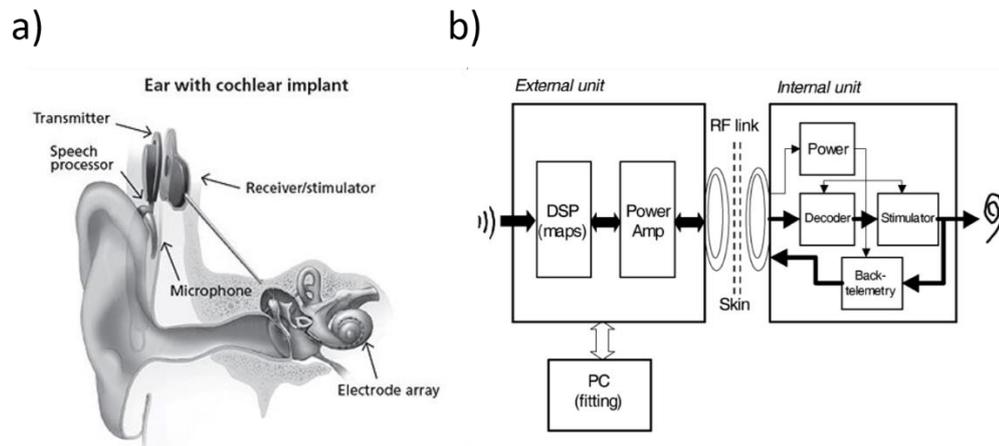


Figure 1.7. (a) A modern cochlear implant system [15], (b) the functional block diagram of a modern cochlear implant system [14].

The speech processor of the cochlear implant should effectively mimic the functions of the normal ear to provide the patients with a hearing experience as natural as possible. Therefore, the operation of the speech is crucial for the hearing of the patients. There are two major units of this operation, namely the front-end processing and sound coding [16]. Many sound coding strategies have been reported in the literature like the advanced combinational encoder (ACE), fine structure processing (FSP), and continuous interleaved sampling (CIS). CIS strategy is the most commonly used sound coding strategy in modern cochlear implant systems. FLAMENCO project utilizes the CIS strategy as well. Figure 1.8 shows the block diagram of the CIS strategy. In this strategy, the output of the microphone is first pre-emphasized to attenuate high frequencies and emphasize low frequencies as the normal conversation covers the frequencies below 1.2 kHz (AGC in Figure 1.8). The output passes through the bandpass filterbank (BPF 1-12 in Figure 1.8) to decompose the speech signal into the different frequency bands. The filtered signals are rectified together with lowpass filtering for the envelope extraction. The envelope signals of wide dynamic range sound are logarithmically compressed into the narrow dynamic range and the biphasic pulse train is modulated by the compressed envelope. The pulse rate is arranged such that there is no overlap across the channels. The current pulses are then directed to the cochlear electrodes.

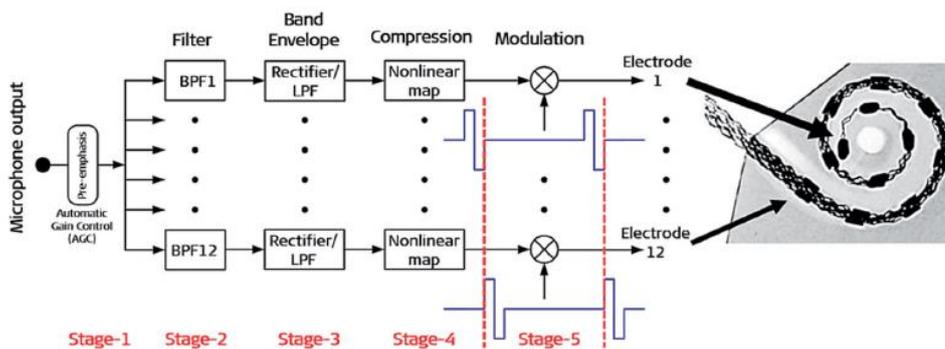


Figure 1.8. The block diagram of the CIS strategy [16].

Although these strategies have produced successful results for the speech processing [17], the drawback is the power consumption of the electrical circuits. The power consumption of the cochlear implants is estimated as 40 mW of which the speech

processor consumes the most [18] while the inner ear consumes only 14  $\mu$ W for the hearing [19]. High power consumption causes regular replacement or recharging of the battery. On the other hand, the speech processor is a bulky component that is located right behind the ear together with a microphone as shown in Figure 1.7 (a). These external components cause several problems for the patients as explained in Section 1.1. Therefore, the miniaturization of the speech processor, eliminating the external microphone, and extending the battery life are the main tasks of the next generation cochlear implants, and the low power fully implantable cochlear implants have the potential to accomplish these tasks.

## **1.5 Fully Implantable Cochlear Implants**

Fully implantable cochlear implants are proposed to eliminate the problems of conventional cochlear implants related to the visible external components and frequent battery recharging. Therefore, the replacement of the microphone with an acoustic transducer, miniaturization of the speech processor, and low power consumption can be considered as the design specifications of the fully implantable cochlear implants.

### **1.5.1 Acoustic Sensors**

The task of microphone replacement was accomplished in modern middle ear implant systems used for the treatment of conductive hearing loss [20]. In these systems, an implantable sensor coupled to the ossicles replaces the microphone and detects the vibration of the ossicles. The output of the sensor is amplified and this signal actuates the stapes to compensate for the hearing loss. Similar to the implantable sensor of the middle ear implants, there are different types of sensors reported in the literature which can be implemented onto the ossicles and replace the microphone of cochlear implants [7], [21], [22].

Young et al. [21] proposed an implantable MEMS accelerometer as a microphone of the cochlear implant. Figure 1.9 (a) presents the system architecture and Figure 1.9 (b) shows the MEMS accelerometer of the system. The interdigitated structure forms parallel capacitors and the sound is sensed through the capacitance change. The accelerometer was placed on the umbo to convert mechanical vibrations to electrical signals. The surface dimensions of the accelerometer are 1 mm x 1 mm which is very suitable for the middle ear volume. However, the sensitivity of the accelerometer is 11.5 mV/g and this requires very low noise operation of the interface electronics to process input signals lower than 60 dB SPL for the frequencies lower than 1 kHz.

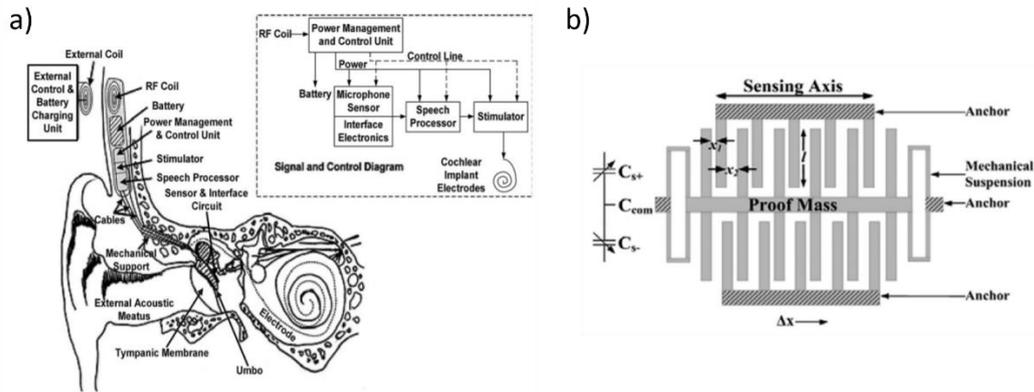


Figure 1.9. (a) The system architecture, (b) accelerometer of [21].

Jia et al. [22] introduced a floating piezoelectric microphone to replace the external microphone of the conventional cochlear implants. Figure 1.10 shows the model of floating piezoelectric microphone. The dimensions of the piezoelectric ceramic are 4 mm x 1 mm x 0.3 mm like a cantilever and this was encapsulated by a hermetically sealed and biocompatible package together with a pre-amplifier chip, lead wires, and a titanium clip. The system was attached to the umbo or the long process of incus during the tests and it was stated that the sensitivity of the system was better when attached to the long process of the incus. The floating piezoelectric microphone achieved a near-flat response and was able to detect the input sound of a minimum of 50 dB SPL. However, the system requires very low noise operation of interface electronics for the frequency band of 1000-3000 Hz and the size of the package is 5.91 mm x 2.4 mm x 2.02 mm which is not convenient for the middle ear volume.

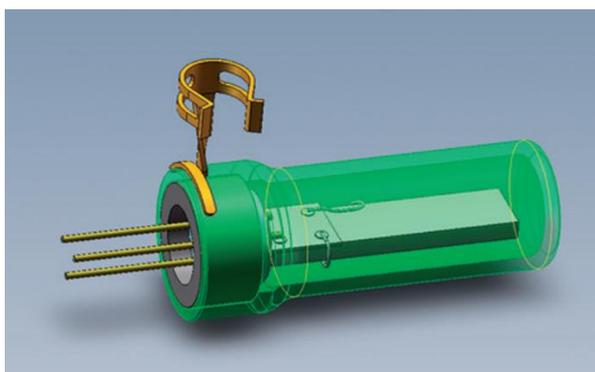


Figure 1.10. The model of floating piezoelectric microphone [22].

Our research group designed a multichannel piezoelectric acoustic transducer to mimic the operation of the cochlea [7]. Figure 1.11 (a) illustrates the concept of the FLAMENCO project and Figure 1.11 (b) shows the multichannel piezoelectric acoustic transducer. The transducer consists of eight cantilevers each of which resonates at different frequencies between 250-5500 Hz such that the transducer mechanically filters the incoming sound. However, although the operation of the transducer was successful at the resonance frequencies of the cantilevers, it was not able to process incoming sound whose frequency was in between the resonances due to very high-Q filtering. Moreover, the size of the transducer ( $5 \times 5 \times 0.6$  mm) is not suitable for the middle ear volume and it is not possible to reconfigure the resonance frequencies and the bandwidths of the cantilevers after the fabrication.

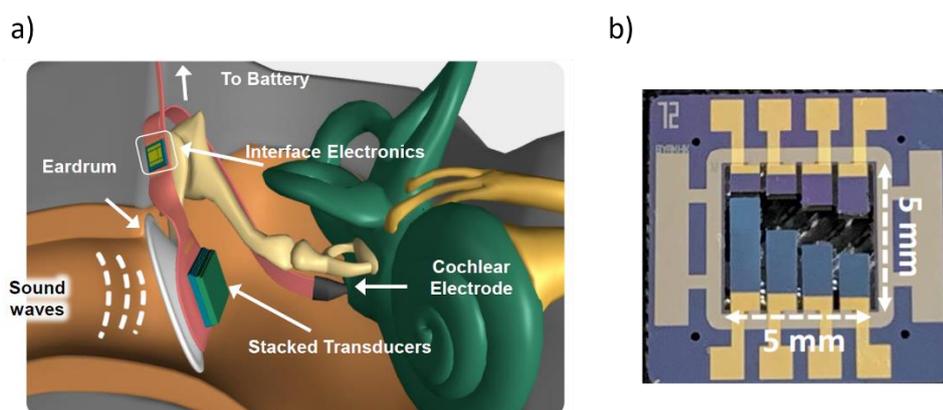


Figure 1.11. (a) The concept of FLAMENCO project, (b) multichannel piezoelectric acoustic transducer [7].

## 1.5.2 Front-End Circuits

The sensors to replace the microphone of the conventional cochlear implants need a front-end circuit for the output of the sensor to be processed effectively. In addition, a well-designed front-end circuit is an important contributor to the goals of the miniaturization and low power operation of the speech processor. The operation of a front-end circuit of a fully implantable cochlear implant would be defined as amplifying low-level signals of the implantable sensor without noise contribution, decomposing the input sound into the specific frequency bands, and setting the voltage level of each channel.

Figure 1.12 shows the alternative methods for the processing blocks of sound coding strategies [23]. Most of the modern cochlear speech processors utilizes digital signal processing (DSP) technology. Therefore, the front end circuit usually consist of pre-amplifiers, analog to digital converters (ADC) and the digital filters. Although the digital technology provides the implant with high reconfigurability through the software, the blocks of ADC and DSP both consume very high power, approximately 5 mW [24], and occupy a larger area which violates the goals of the miniaturization and low power operation of the speech processor. Therefore, utilizing subthreshold analog blocks for the front-end and filtering operation of the speech processor would be a promising solution for the fully implantable cochlear implants to achieve low power consumption and miniaturization.

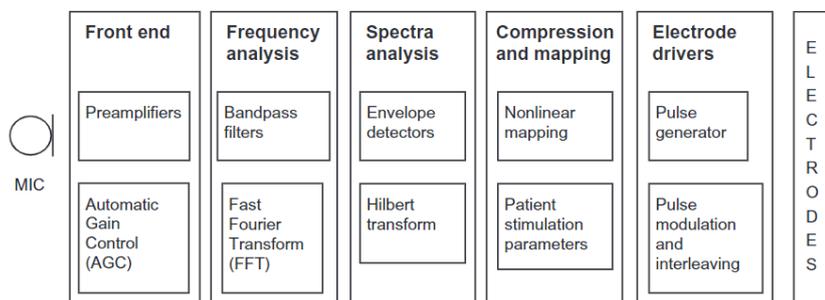


Figure 1.12. The modules and processing methods for sound coding [23].

Georgiou et al. [25] used low-power analog circuits for the signal processing and digital circuits for the robust communication of the cochlear implant. Figure 1.13 (a) shows the block diagram of the proposed cochlear implant system and Figure 1.13 (b) describes the analog operations of the speech processor. The system consists of two sets of eight parallel channels and utilizes the CIS strategy for sound coding. The active area of the chip was  $3.5 \times 6 \text{ mm}^2$  and all blocks were encapsulated in a hermetically sealed platinum case. The power consumption of the chip was measured as  $126 \mu\text{W}$ , excluding the blocks of biphasic pulse stimulus. The size and power consumption of the chip show the potential of analog processing in terms of miniaturization and low power operation of the speech processor. However, as the sound waves are captured by an external microphone, the system is not suitable for the FICI concept.

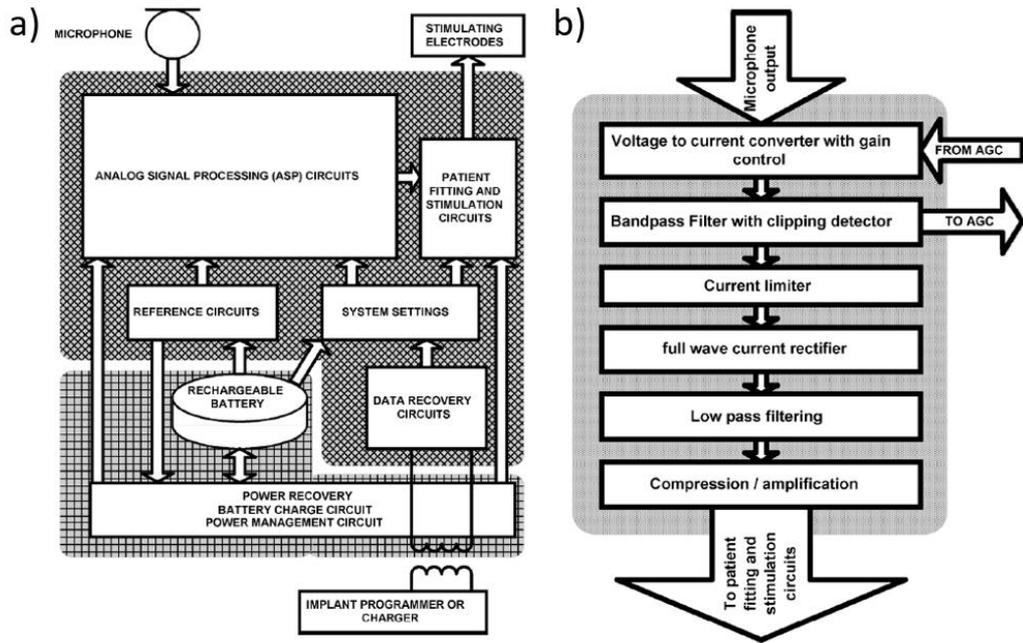


Figure 1.13. (a) The block diagram of the cochlear implant, (b) analog operations of the system [25].

Yip et al. [6] proposed a fully implantable cochlear implant system on a chip with a piezoelectric middle ear sensor. The block diagram of the system is shown in Figure 1.14. As the system utilizes an implantable piezoelectric sensor that replaces the

external microphone, the first block of the SoC is the front-end for the sensor. A charge amplifier interfaces with the piezoelectric sensor and a programmable gain amplifier sets the voltage level of the sensor output. The signal is then converted to the digital domain through the ADC to process the sound with FIR filters. The chip area is  $3.6 \times 3.6 \text{ mm}^2$  and the system consumes  $572 \mu\text{W}$  in 8-channel mode, including the stimulation. Although this system satisfies the requirements of a FICI such as having an implantable sensor, miniaturized and low power speech processor, the power consumption and programmability of the system could be further optimized through analog subthreshold filters.

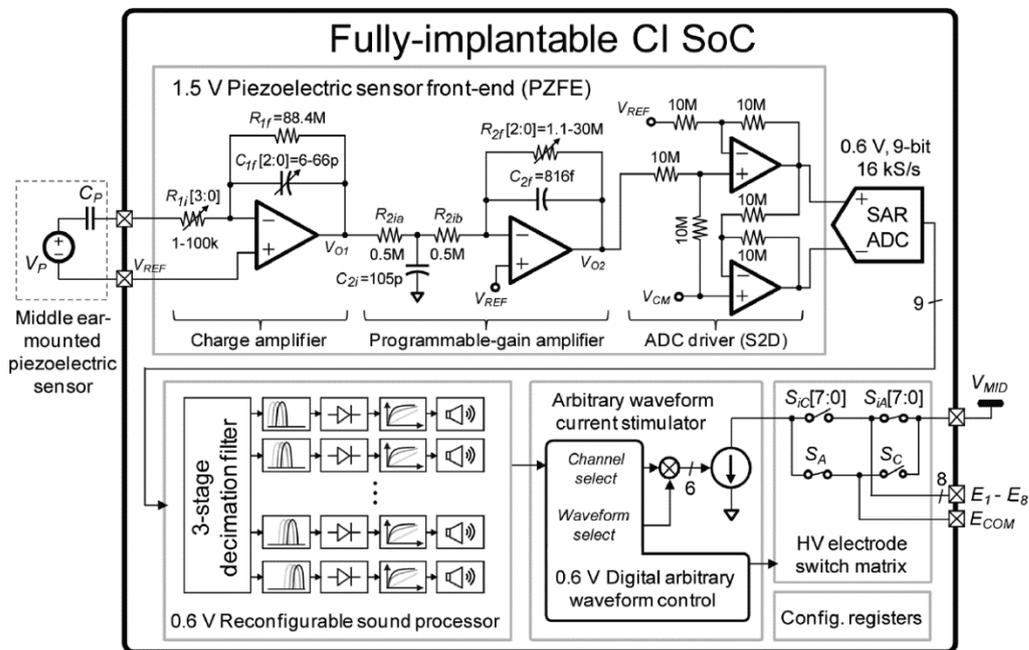


Figure 1.14. The block diagram of FICI system [6].

Uluşan et al. [26] designed an interface electronics for the multichannel acoustic transducer of the FLAMENCO project. The block diagram of the interface electronics is presented in Figure 1.15. As the sound is filtered mechanically by the piezoelectric cantilever array, there is no electrical filtering in this design which reduces the power consumption. To process low-amplitude signals of the transducer, the front-end circuit starts with the logarithmic amplifier array. The system further processes the signal based on the CIS strategy in the analog domain. The power

consumption of the front-end is  $51.2 \mu\text{W}$  thanks to analog processing and the chip area is  $1.4 \times 1.4 \text{ mm}^2$ . Although the interface electronics has a better performance in terms of power consumption and chip area compared to the highlighted designs, the system is not able to provide the cochlear implant with high programmability and achieve an ideal frequency response for natural auditory perception.

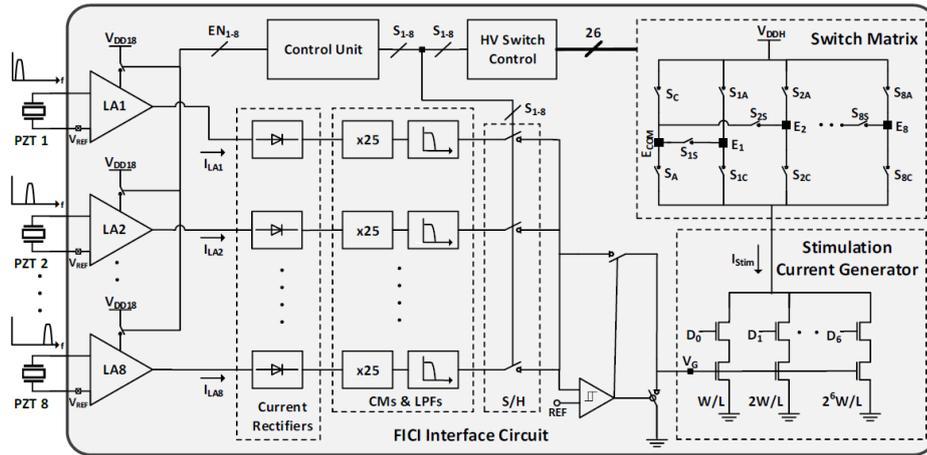


Figure 1.15. The block diagram of interface electronics [26].

## 1.6 Objectives of the Thesis

The main objective of this thesis is to design and implement a low-power, highly programmable analog front-end circuit for fully implantable cochlear implants. By adopting the best of the highlighted front-ends such as analog signal processing, high programmability through digital control blocks and interface electronics for an implantable acoustic sensor, the system achieves all the objectives to construct a fully implantable cochlear implant system which embodies replacement of the external microphone, miniaturization and low power operation of the speech processor. This work has been completed as a part of the FLAMENCO Project. Considering the requirements for an ideal fully implantable cochlear implant, the design specifications are identified as follows:

1. **Low Noise Operation:** The analog front-end is designed to interface with the single-channel piezoelectric acoustic transducer. Since the transducer operates in the non-resonance region, the output level is very low for the weak inputs. Therefore, the system should have very low input-referred noise to process the low voltage outputs of the transducer with the desired signal-to-noise ratio (SNR) which determines the hearing threshold level of the system. It is determined that input-referred noise of each channel should be lower than  $20 \mu\text{V}_{\text{rms}}$  within the passband.
2. **Ideal Frequency Response:** The system should decompose an incoming sound into specific frequency bands through a filter bank. To provide a near-natural hearing, the filter bank should set the most efficient combination of the channel number, center frequencies, and bandwidths of the channels. It is determined that a 12-channel operation is required within the acoustic band of 85-6500 Hz with the quality factors of 1-4.
3. **High Programmability:** There might be faulty channels after the implantation or the performance of some channels might decrease over time due to the increase in the impedance. In such cases, the remaining channels should compensate for the lost bands of the faulty channels. Therefore, the center frequency and bandwidth of each channel should be programmable. In addition, for compatibility with different resonance frequencies of the acoustic transducers, the bandwidth of LNA should be tunable. Moreover, to provide the system with the ability to amplify specific frequencies, the voltage level of each channel should be reconfigurable through the gain of the variable gain amplifiers.
4. **Low Power Consumption:** The power consumption of the speech processor directly affects the lifetime of the battery. The high power consumption causes frequent battery recharging. Therefore, the power consumption of the analog front-end should be as low as possible to extend the battery life. It is determined that the power consumption of the system should be lower than  $10 \mu\text{W}$  while all channels are operating.

5. **Area Efficiency:** The external speech processor of the conventional cochlear implants should fit into the middle ear volume. Therefore, the speech processor should be miniaturized and there should be no external bulky components if possible. It is determined that the analog front-end circuit should occupy an area smaller than  $2 \text{ mm}^2$ .

## 1.7 Organization of the Thesis

The rest of the thesis is organized as follows:

**Chapter 2** covers the design of a low-power, highly tunable, biquadratic Gm-C bandpass filter as a part of the analog front-end circuit. The chapter starts with overviews on the continuous-time filters and operational transconductance amplifier (OTA) structures in the literature. After examining the design specifications, the chapter continues with the circuit design and analysis of the proposed bulk-driven subthreshold folded cascode OTA cell and 2<sup>nd</sup> order programmable Gm-C bandpass filter. The performance of the filter is evaluated through the experimental results at the end.

**Chapter 3** presents the design of ultra-low-power highly programmable analog front end circuit for fully implantable cochlear implants. The chapter starts with the design specifications of the system. In the circuit design and analysis part, the building blocks of the analog front end circuit which are LNA, filter bank, VGA, and control block are reviewed. The simulation results of the blocks and overall operation together with the discussions on the results are presented at the end.

**Chapter 4** concludes the thesis with the contributions and achievements of the design and discusses the future work to improve the performance of the analog front-end circuit.



## CHAPTER 2

### LOW-POWER HIGHLY TUNABLE BIQUADRATIC $G_m$ -C BANDPASS FILTER

#### 2.1 Motivation

The cochlea decomposes incoming sound waves into approximately 3500 frequency bands [27]. This number corresponds to the number of healthy hair cells located throughout the cochlea. In case of damaged or lost hair cells, the frequency selectivity should be realized artificially by the speech processor of the cochlear implant to mimic the operation of the cochlea. Therefore, the filtering performance of the speech processor is of great importance. Even though the filtering operation is realized in the digital domain for the programmability in conventional cochlear implants, a different approach is studied in this thesis by implementing analog filters to decrease the power consumption and miniaturize the speech processor while providing the implant with programmability like in the digital domain so that the design is compatible with the fully implantable cochlear implants.

There are two main categories in continuous time filter design: active and passive filters. A passive filter employs passive elements such as resistors, capacitors, inductors, and, transformers while an active filter employs active blocks like operational amplifier (OPAMP) and operational transconductance amplifiers (OTA). Although the filter design with passive elements is easier, the bulky inductors or capacitors should not be employed in the speech processor of the fully implantable cochlear implants due to large on-chip area. The active-RC filters usually require a high-gain operational amplifiers (OPAMP) causing high power consumption and are not programmable which is not desirable for the operation of the fully implantable cochlear implants [28]. On the other hand,  $G_m$ -C filters have the potential to provide tunability while achieving low power consumption [29], [30]. Therefore, the design

of a low-power, highly tunable  $G_m$ -C bandpass filter is determined as the first step of the proposed analog front-end design for the fully implantable cochlear implants.

This chapter presents the design and implementation of the low-power highly tunable biquadratic  $G_m$ -C bandpass filter. There are four OTA cells and two capacitors in the proposed second-order bandpass filter to form an active inductor, active resistor, and attenuator. The bias currents to the OTA cells and capacitances are utilized to set the center frequency and bandwidth of the filter. The transistors in the OTA cells operate in the weak inversion region to achieve low power consumption. The input transistors of the OTA cells are driven from the bulk to reduce the transconductance of the OTA to cover the low frequencies of the acoustic band. Although the reduction in the transconductance decreases the gain, this is compensated by increasing output resistance with folded cascode structure.

Section 2 and 3 provide a brief overview of the continuous-time analog filters and operational transconductance amplifiers respectively. In Section 4, the design specifications of the proposed bandpass filter are explained. The proposed OTA cell and filter topology are analyzed in Section 5. In the end, the experimental results of the fabricated filter chip are presented in Section 6, and the results are discussed in Section 7.

## **2.2 Overview of Continuous Time Filters**

An electronic filter ideally passes electrical signals in a certain frequency range without any loss while suppressing signals with other frequencies. Therefore, the filter characteristics are defined by the transfer function which is the ratio of the Laplace transforms of the output and input signals to show the frequency domain behavior of the filter. Based on the frequency response, the filters are categorized as low pass, high pass, bandpass and, bandstop filters as shown in Figure 2.1.

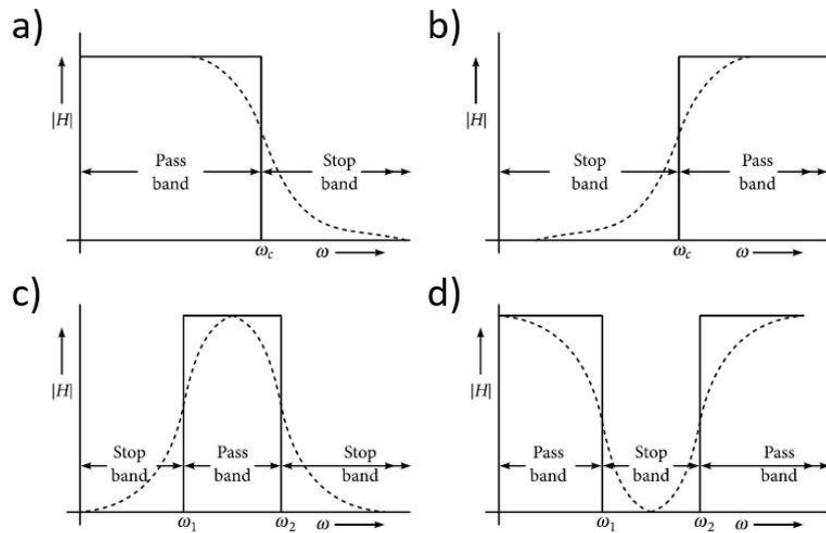


Figure 2.1. The frequency responses of the filter types: a) lowpass, b) highpass, c) bandpass, d) bandstop filters [31].

There are several parameters to explain the frequency response of the filter. The cut-off frequency (or -3 dB frequency) is defined as the frequency at which the output gain decreases by 3 dB from its maximum value which corresponds to half of the maximum power. The center frequency is the frequency that lies at the center of the lower and upper cut-off frequencies. The bandwidth of the filter is defined as the band of frequencies in between the lower and upper cut-off frequencies and calculated as the difference between cut-off frequencies. The quality factor ( $Q$ ) of the filter is the measure of the filter selectivity and is calculated as the ratio of the center frequency over bandwidth.

Low pass filters (LPF) suppress the signals whose frequencies are above the cut-off frequency of the filter ( $\omega_c$ ) and pass the signals within the bandwidth with constant gain. The high pass filters (HPF), on the other hand, suppress all of the frequencies below the cut-off frequency and pass the frequencies above the cut-off frequency. LPFs and HPFs are widely used to eliminate the high-frequency and low-frequency noises respectively. Bandpass filters (BPF) allow the frequencies in the passband to pass through and attenuate the signals whose frequency is in the stopband. BPFs are greatly used in audio signal processing, especially in the speech processor of

cochlear implants. Bandstop filters (BSF) are the complement of BPFs which rejects the signals in between the cut-off frequencies. BSFs are extensively used to reduce the line noise in telephonic signal transmission [31].

There are three types of electronic filters that are most commonly used: continuous-time (Analog) filters, digital filters, and sampled-data filters. In digital filters, the analog input signal is converted to the digital equivalent by using an ADC and processed in the digital domain. The filtered signal is converted back to the analog form by using a DAC. The sampled data filters can be assumed as the hybrid of the analog and digital filters. These filters are not continuous in time but continuous in signal value [32]. The switched-capacitor filters are an example of sampled data filters and usually require a high gain opamp. However, the additional blocks of ADC and DAC in digital filters and high gain opamp in switched-capacitor filters cause a higher power consumption compared to the continuous-time filters [33]. Therefore, continuous-time filters become a better option for fully implantable cochlear implant applications as long as these filters provide the implant with programmability and occupy a smaller area as well. The continuous-time filters are divided into two categories as passive and active filters.

The passive elements of resistor, capacitor and inductor have been extensively used to form passive filters [31]. Figure 2.2 shows the typical second-order passive low pass filter circuit consisting resistor, capacitor, inductor and equation (2.1) gives the corresponding transfer function of the filter where the center frequency and quality factor of the filter are equal to  $\omega_0^2=1/LC$  and  $Q=\omega_0L/R$  respectively. The main advantage of the passive filters is that these filters do not need a power source to operate. However, the passive components are not able to amplify the input signal. In addition, it is not convenient to utilize a passive filter in fully implantable cochlear implant applications since the inductance or capacitance should be high to cover the low frequencies of the acoustic band. To achieve high values of capacitor or inductor, they should occupy a large on-chip area which violates the goal of miniaturization of the speech processor.

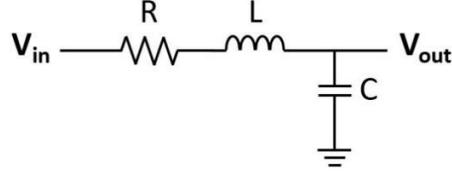


Figure 2.2. A typical second-order passive low pass filter.

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \quad (2.1)$$

The replacement of the inductor forms the basis for the design of the active filters. These filters contain active blocks in combination with resistors and capacitors to show an RLC filter performance, especially at low frequencies. There are two active blocks that are widely used in active filters. If the active block is an OPAMP, the filter is named as an active-RC filter. Figure 2.3 depicts a simple structure of active-RC low pass filter which is known as unity gain Sallen-Key low pass filter [34]. Equation (2.2) gives the transfer function of the structure and equation (2.3) gives the cut-off frequency and quality factor of the filter. Although active-RC filters are able to eliminate the problems of the passive filters related to large inductors for low-frequency operation and amplification without significant size increase, it is not easy to electronically program the active-RC filter parameters which is not convenient for the patient fitting applications of the fully implantable cochlear implants.

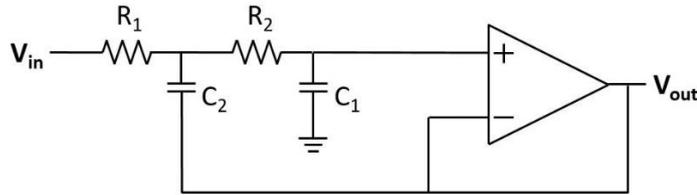


Figure 2.3. The structure of unity gain Sallen-Key low pass filter [34].

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{s^2 + \left(\frac{1}{R_2 C_1} + \frac{1}{R_1 C_1}\right)s + \frac{1}{R_1 C_1 R_2 C_2}} \quad (2.2)$$

$$w_0^2 = \frac{1}{R_1 C_1 R_2 C_2}, \quad Q = \frac{\sqrt{R_1 C_1 R_2 C_2}}{(R_1 + R_2) C_2} \quad (2.3)$$

The implementation of OTAs as the active block of the active filters would eliminate the programmability issue of the active-RC filters and achieve low power consumption through the subthreshold operation. Therefore, Gm-C filters are the best option for the acoustic filter bank of fully implantable cochlear implants. It is possible to form active inductors and resistors by using OTAs and capacitors in order to realize bandpass filters. The most common method to form an active inductor is based on the principle of the gyrator which can be constructed by using OTAs. A gyrator act as the complement of the transformer such that the current in one port is proportional to the voltage across the other port as summarized in Figure 2.4 [35].

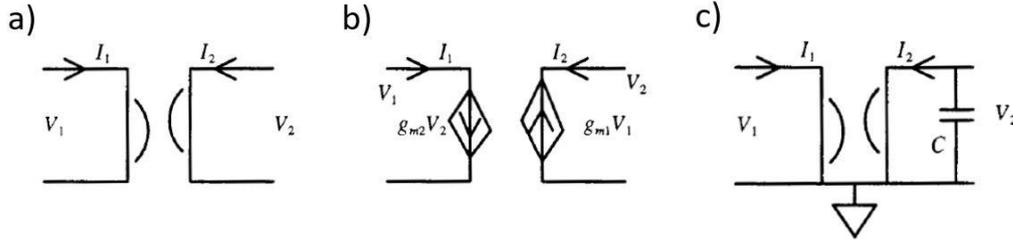


Figure 2.4. a) The symbol of gyrator, b) small signal model of gyrator, c) grounded inductor formed by gyrator and capacitor [35].

When there is a capacitor added to the output of a gyrator, the inductive behavior can be obtained as follows:

$$\frac{V_1}{I_1} = \frac{V_1}{g_{m2}V_2} \quad (2.4)$$

$$V_2 = \frac{-I_2}{sC} = \frac{g_{m1}V_1}{sC} \quad (2.5)$$

Substituting for  $V_2$  from equation (2.5) into (2.4):

$$\frac{V_1}{I_1} = \frac{V_1}{g_{m2}(\frac{g_{m1}V_1}{sC})} = \frac{sC}{g_{m2}g_{m1}} = sL, \quad L = \frac{C}{g_{m2}g_{m1}} \quad (2.6)$$

It is possible to form an active resistor to be used while constructing a  $G_m$ -C bandpass filter by connecting the output of OTA to the inverting terminal of OTA as shown in Figure 2.5 (b) [35].

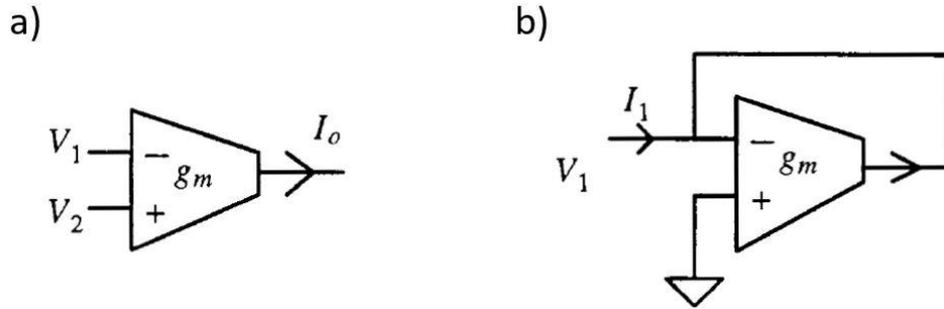


Figure 2.5. a) The symbol of OTA, b) active grounded resistor formed by OTA [35].

The resistive behavior can be extracted as follows:

$$I_1 = g_m V_1 \quad (2.7)$$

$$\frac{V_1}{I_1} = R = \frac{1}{g_m} \quad (2.8)$$

Equations (2.6) and (2.8) show that the inductance and resistance can easily be tuned through the values of transconductances. The transconductance can be controlled by the bias current to the OTA cell. Thus, it is possible to reconfigure the center frequency and bandwidth of  $G_m$ -C bandpass filter through the bias currents which is an important parameter for the patient fitting applications of the fully implantable cochlear implants [35].

The basic building blocks of a  $G_m$ -C filter are the  $G_m$ -C integrator and biquads. A  $G_m$ -C integrator can be formed by adding a capacitor to the output of the transconductor as shown in Figure 2.6 [36]. The output voltage of the circuit is calculated as in the equation (2.9). The unity-gain frequency ( $\omega_0$ ) of the integrator is obtained as  $G_m/C_L$ . As a result, the output voltage is equal to the multiplication of the integrator's unity-gain frequency and the integration of the input voltage.



Equations (2.11)-(2.13) summarize the programmability potential of  $G_m$ -C bandpass filters. By tuning the transconductances of OTA cells, the center frequency, quality factor, and gain of the filter can easily be reconfigured. When the transconductances of the cells are small enough, the capacitances would be small as well to achieve low frequencies which occupy a small on-chip area. Thus,  $G_m$ -C bandpass filters become an ideal candidate for the acoustic signal processing of the fully implantable cochlear implants as these filters accomplish the tasks of programmability and miniaturization of the speech processor. The only remaining task for  $G_m$ -C bandpass filters is to achieve low power operation. This would be realized by well-designed subthreshold OTA cells.

### 2.3 Overview of Operational Transconductance Amplifiers

An OTA is a voltage-controlled current source as the output current is proportional to the differential input voltage. The main difference between OTAs and OPAMPs is the output resistance. OPAMPs have low output resistance and act as voltage-controlled voltage sources while OTAs have high output resistance. Therefore, it is better to use OTAs when the output load is capacitive as in the filters. However, the linearity performance of OTAs is worse than the linearity performance of OPAMPs as OTAs operate in an open-loop configuration. The main advantage of OTAs is that it is possible to control the transconductance through the external bias current or voltage in filter applications.

There are three conventional OTA topologies: two-stage OTAs, telescopic OTAs and folded cascode OTAs. Figure 2.8 illustrates the two-stage OTA structure. In this topology, Q1 and Q2 are the input differential pair that converts the input voltage to the current. The bias current  $I_{ref}$  is mirrored through the transistors of Q3-Q4-Q5-Q7-Q8. There is a second stage amplifier which is formed by the transistors of Q6-Q7 and cascaded to the first stage [37].

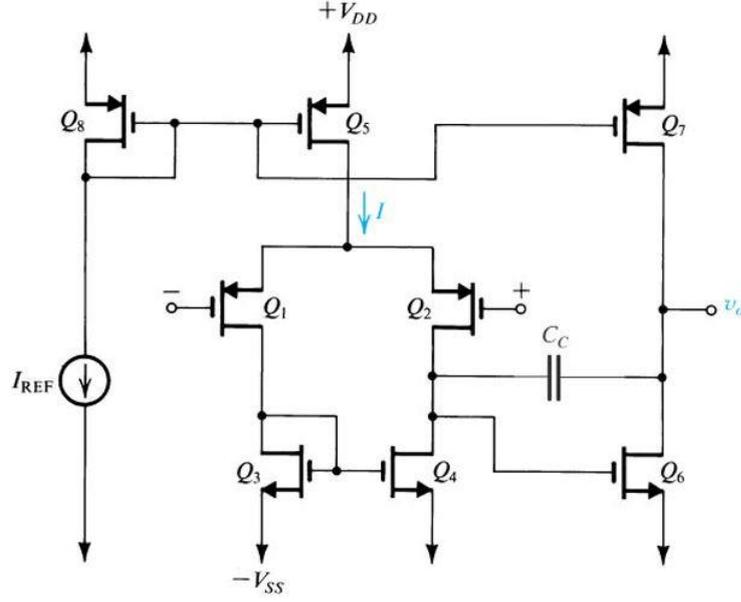


Figure 2.8. The topology of two-stage OTA [37].

The gain, input and output resistance of the two-stage OTA can be extracted from the small-signal model shown in Figure 2.9 as follows:

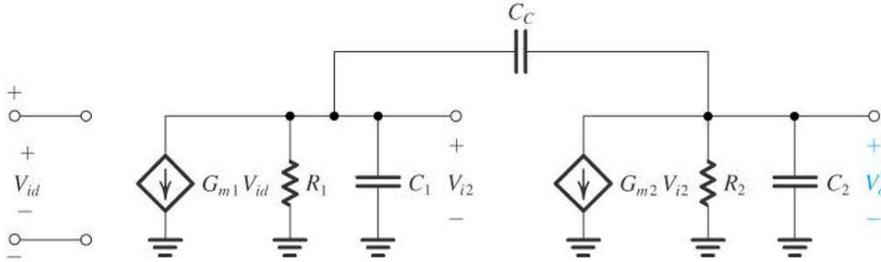


Figure 2.9. The small signal model of two-stage OTA [37].

$$A_v = g_{m2}g_{m6}(r_{o2}/r_{o4})(r_{o6}/r_{o7}) \quad (2.14)$$

$$R_{in} = \infty \quad (2.15)$$

$$R_{out} = r_{o6}/r_{o7} \quad (2.16)$$

Although this topology provides a higher gain and has high output voltage swing compared to single-stage OTA, the power consumption of the structure is higher due to the second stage and the input common-mode range is small for higher bias currents.

The issue of high power consumption in a two-stage OTA structure would be eliminated by using a telescopic structure. A conventional telescopic OTA topology is shown in Figure 2.10. The topology consists of differential input pair (M1 and M2), cascode transistors (M3 and M4), and active loads (M5-M8). The cascode transistors and active loads increase the output resistance of the telescopic OTA which results in an increase in the gain [38]. The gain, input and output resistance of the structure are calculated as follows:

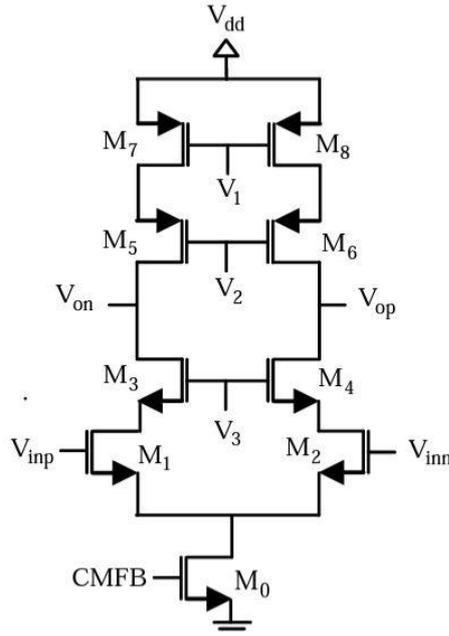


Figure 2.10. The topology of telescopic OTA [38].

$$A_v = g_{m1}[(g_{m5}r_{o5}r_{o7})/(g_{m3}r_{o3}r_{o1})] \quad (2.17)$$

$$R_{in} = \infty \quad (2.18)$$

$$R_{out} = (g_{m5}r_{o5}r_{o7})/(g_{m3}r_{o3}r_{o1}) \quad (2.19)$$

Although telescopic OTA topology is able to provide high gain thanks to an increase in the output resistance through cascode transistors and achieve low power consumption, the output swing of the telescopic OTA is limited compared to the two-stage OTA topology.

A folded cascode OTA is able to overcome the drawback of limited output swing in the telescopic OTA. A conventional folded cascode OTA is illustrated in Figure 2.11. The transistors of M1 and M2 are the differential input pair. Depending on the application, the pair would be n-type or p-type. For example, it is better to use p-type input pair for applications that require small transconductance as PMOS has smaller transconductance compared to NMOS. For the applications which require a high-speed operation, it is logical to use n-type input pair since NMOS has higher carrier mobility. As the cascode part of the topology is similar to telescopic OTA, the output resistances and thereby the gains are roughly equivalent [39].

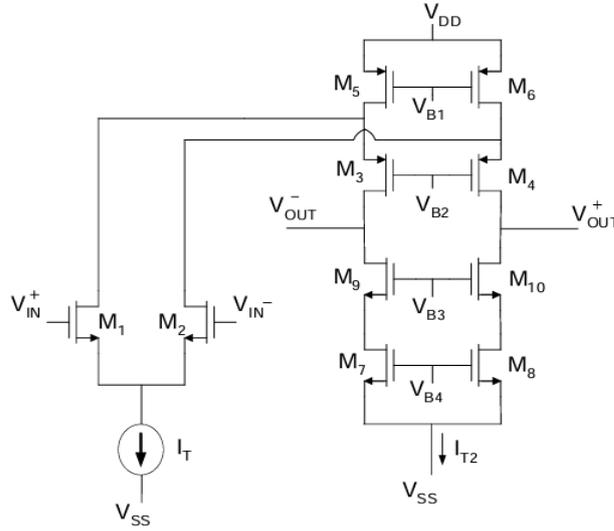


Figure 2.11. The topology of folded cascode OTA [39].

$$A_v = g_{m2}[(g_{m10}r_{o10}r_{o8})/(g_{m4}r_{o4}(r_{o2}/r_{o6})] \quad (2.20)$$

$$R_{in} = \infty \quad (2.21)$$

$$R_{out} = (g_{m10}r_{o10}r_{o8})/(g_{m4}r_{o4}(r_{o2}/r_{o6})) \quad (2.22)$$

Although the folded cascode structure has a better input and output swing range, the folded cascode structure consumes more power compared to the telescopic OTA. In addition, the gain is lower than the one in the two-stage OTA. Therefore, the folded cascode OTA would be treated as a compromise between the two-stage OTA and telescopic OTA.

## 2.4 Design Specifications

Considering the advantages and disadvantages of each filter and OTA topology, it is determined to design a  $G_m$ -C bandpass filter with folded cascode OTA cells for acoustic signal processing. The main goal of this design is to prove that the proposed filter is able to overcome the bottlenecks of the multichannel acoustic transducer [7]. That is why a filter block is designed first instead of a complete analog front-end. The success of the proposed filter would be a prerequisite for the design of the analog front-end. In order for the proposed filter to be both comparable with the acoustic transducer and ideal for a fully implantable cochlear implant system and, the design parameters are determined as follows:

To compare the performance of electrical filtering of the proposed filter with the mechanical filtering of the acoustic transducer of FLAMENCO accurately, the channel number, target frequency band, and the center frequencies of the channels should be the same. Thus, the filter should be able to cover the acoustic band of 300-5500 Hz with eight resonance frequencies. Different from the acoustic sensor, the bandwidths of the channels should be wide enough to cover the frequencies in between the resonances. In addition, the center frequencies and bandwidths of the channels in the proposed filter should not be fixed but programmable so that the speech perception would be maximized for each individual.

The main advantage of mechanical filtering is that there is no power consumption. As the electrical filtering replaces the mechanical filtering in the proposed system, the filter introduces an additional power consumption to the fully implantable cochlear implant. Therefore, it is crucial to have low power consumption in order to extend the battery life of the implant. It is determined that the power consumption of the filter should not be higher than  $0.5 \mu\text{W}$  so that the eight-channel filter bank does not consume power higher than  $5 \mu\text{W}$ .

The speech processor should fit into the middle ear volume in a FICI. Therefore, the on-chip area of the filter should be as low as possible. It is determined that the on-

chip area of the filter should not be larger than  $0.1 \text{ mm}^2$  so that a filter bank with the proposed filter for an 8-channel speech processor does not occupy an on-chip area larger than  $1 \text{ mm}^2$ .

The filter would interface with a single-channel acoustic transducer. As the transducer would operate in non-resonant mode, the output level of the transducer would be very low. Therefore, the input-referred noise of the filter should be much lower than the output of the transducer. On the other hand, the linear range of the filter should handle the high-level inputs. Referring to the sensitivity levels of commercial accelerometers, it is determined that the input-referred noise of the filter should be lower than  $50 \mu\text{V}_{\text{rms}}$  and the filter should stay linear up to  $100 \text{ mV}_{\text{rms}}$ .

## **2.5 Circuit Design and Analysis**

### **2.5.1 Bulk-driven Subthreshold Folded Cascode OTA**

The performance of the  $G_m$ -C bandpass filter is in strong relation with the performance of OTA cells that form the filter. The filter should cover the acoustic band of 300-5500 Hz. In order to cover the low frequencies of this band, the transconductances of OTA cells should be low enough or the capacitances should be high enough as indicated in equation (2.11). However, as the capacitors with high capacitances occupy a large on-chip area, OTA cells with very small transconductances are preferable. In addition, since the power consumptions of OTA cells determine the power consumption of the filter, low power operation is crucial for the OTA cells. Therefore, a small transconductance and low power operation are the most important parameters for the OTA in our application.

To achieve low power operation, the transistors of OTA would operate in the subthreshold region (weak inversion). In this region, the supply voltage is less than the threshold voltage of the transistor ( $V_{\text{th}}$ ). The inversion layer is not formed yet when the gate-to-source voltage ( $V_{\text{gs}}$ ) is less than the threshold voltage. However,

the diffusion of the minority carriers between drain and source terminals causes the subthreshold leakage current. As this current is the operating current of the device in the subthreshold region, the drain current is very low compared to the drain current in the strong inversion [40]. The drain current in the subthreshold region is given as follows [41]:

$$I_{D,sub} = \begin{cases} I_0 e^{\frac{V_{gs}-V_{TH}}{n\phi_t}} \left( 1 - e^{-\frac{V_{ds}}{\phi_t}} \right), & V_{ds} < 3\phi_t \\ I_0 e^{\frac{V_{gs}-V_{TH}}{n\phi_t}}, & V_{ds} > 3\phi_t \end{cases} \quad (2.23)$$

where  $\phi_t$  denotes the thermal voltage and equals to  $kT/q$  ( $\phi_t=26$  mV @300K).

$I_0$  is the drain current when the gate-to-source voltage is equal to the threshold voltage and given by:

$$I_0 = \mu_0 C_{ox} \frac{W}{L} (n-1) \phi_t^2 \quad (2.24)$$

where  $\mu_0$  represents the carrier mobility,  $C_{ox}$  denotes the gate-oxide capacitance,  $W$  and  $L$  shows the width and length of the channel respectively and  $n$  is the subthreshold slope factor.

Similar to the strong inversion, the subthreshold region would be divided into two subregions based on the equation (2.23). When the drain-to-source voltage ( $V_{ds}$ ) is lower than the three times the thermal voltage, the drain current exponentially depends on the drain-to-source voltage. This subregion would be named the non-saturation region. When the drain-to-source voltage is higher than the three times the thermal voltage, the dependence of the drain current on the drain-to-source voltage would be ignored and the drain current would be modulated by gate-to-source voltage ( $V_{gs}$ ). This subregion would be called as the saturation region. Figure 2.12 summarizes the drain current characteristics depending on the drain-to-source voltage in the subthreshold region. Thus, the supply voltage would be reduced and the transistors of OTA cell would operate in the subthreshold region as long as the drain-to-source voltages are lower than the three times the thermal voltage [40], [41].

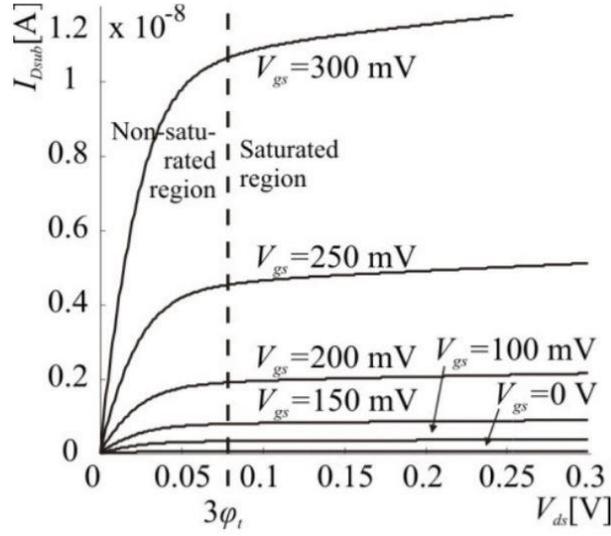


Figure 2.12.  $I_D$ - $V_{ds}$  characteristics of subthreshold region [41].

Having small transconductance is another important parameter for the OTA in our application to cover low frequencies of the acoustic band. To decrease the transconductance, the input pair of OTA would be driven from the bulk terminal as shown in Figure 2.13 [42]. When the bulk voltage is not equal to the source voltage, the body effect occurs in MOSFETs. This effect increases the threshold voltage and lowers the voltage headroom [43]. However, when the bulk is biased such that the bulk-to-source voltage becomes positive, it causes a reduction in the threshold as indicated in equation (2.25).

$$V_{TH} = V_{T0} + \gamma(\sqrt{|2\Phi_f| - V_{BS}} - \sqrt{|2\Phi_f|}) \quad (2.25)$$

where  $\gamma$  is the Body effect coefficient and  $\Phi_f$  is the Fermi level potential.

On the other hand, when MOSFET is biased such that the inversion layer is formed between the drain and source terminals, the drain current would be modulated by changing the threshold voltage which can be controlled by the bulk voltage. However, the junction diode should not be turned on while driving the transistor from the bulk [42]. Thus, even though a certain bias voltage might be required to keep the junction diode off, the bulk terminal would be an input port and AC signals can be applied to the bulk as input [43].

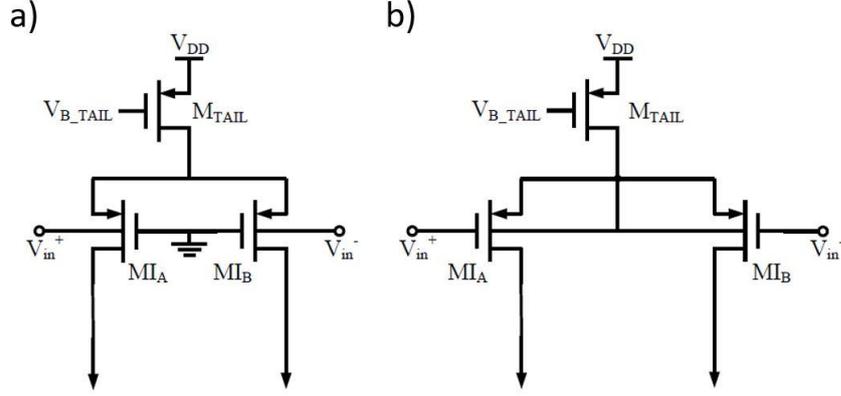


Figure 2.13. a) A bulk-driven and b) a gate-driven PMOS differential pair [42].

The advantage of the bulk-driving technique for our application is that the bulk transconductance is typically three to five times smaller than the gate transconductance [44]. The relation between the gate transconductance and bulk transconductance can be derived from the subthreshold current, equation (2.23), and threshold expressions, equation (2.25), as follows:

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{I_D}{nV_t} = -\frac{\partial i_D}{\partial v_{TH}} \quad (2.26)$$

$$g_{mb} = \frac{\partial i_D}{\partial v_{BS}} = \frac{\partial i_D}{\partial v_{TH}} \frac{\partial v_{TH}}{\partial v_{BS}} \quad (2.27)$$

The terms in the extension of equation (2.27) are calculated as follows:

$$\frac{\partial i_D}{\partial v_{TH}} = -g_m \quad (2.28)$$

$$\frac{\partial v_{TH}}{\partial v_{BS}} = -\frac{\gamma}{2\sqrt{|2\Phi_f| + |V_{BS}|}} \quad (2.29)$$

The derivative of the threshold voltage with respect to the bulk-to-source voltage is a constant which varies from 0.2 to 0.4 depending on the bulk-to-source voltage and process parameters [44]. When the equations (2.28) and (2.29) are combined in the equation (2.27), the bulk transconductance is calculated as three to five times lower than the gate transconductance. However, the reduction in the transconductance causes the reduction in the gain as a drawback of the bulk-driving technique.

Taking the parameters of small  $g_m$  and low power operation for our application into consideration, a bulk-driven folded cascode OTA shown in Figure 2.14 that operates in the subthreshold region is designed as the building block of the  $G_m$ -C filter [45].

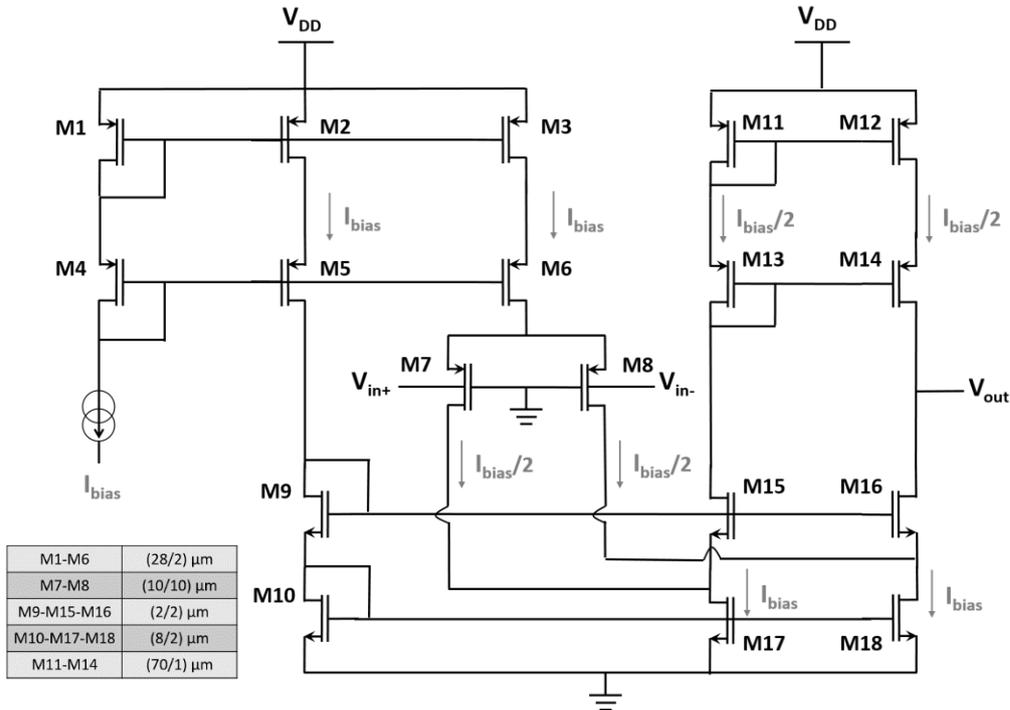


Figure 2.14. The proposed bulk-driven folded cascode OTA.

In this design, the transistors of M7 and M8 are the PMOS differential input pair which are driven from the bulk terminal. The gate terminals of the pair are grounded to ensure that the inversion layer is formed between the drain and source terminals. A DC bias voltage of 500 mV is applied to the bulk terminals of the pair in order to keep the junction diode off so that there is no leakage current. The input bias current is mirrored to the output biasing branch and the sources of the input pair through the transistors of M1-M6. The M9 and M10 provide the DC bias voltages to the M15-M16 and M17-M18 respectively. The transistors of M11-M14 form the cascode load to increase the output resistance for the gain. In this way, the reduction in the gain due to the reduction in the transconductance would be compensated by increasing output resistance as equations (2.30) and (2.31) show. All transistors in the design operate in the subthreshold region for low power consumption.

$$R_{out} = g_{m16}r_{o16}(r_{o8} // r_{o18}) // g_{m14}r_{o14}r_{o12} \quad (2.30)$$

$$A_v = g_{mb8}[g_{m16}r_{o16}(r_{o8} // r_{o18}) // g_{m14}r_{o14}r_{o12}] \quad (2.31)$$

The proposed OTA was designed and simulated in TSMC 0.18  $\mu\text{m}$  CMOS technology. The frequency response of the OTA for the bias current of 40 nA, supply voltage of 1 V, and load capacitance of 1 pF is depicted in Figure 2.15. The simulation result shows that the unity-gain bandwidth of the OTA is 21 kHz and the phase margin is  $81.7^\circ$ .

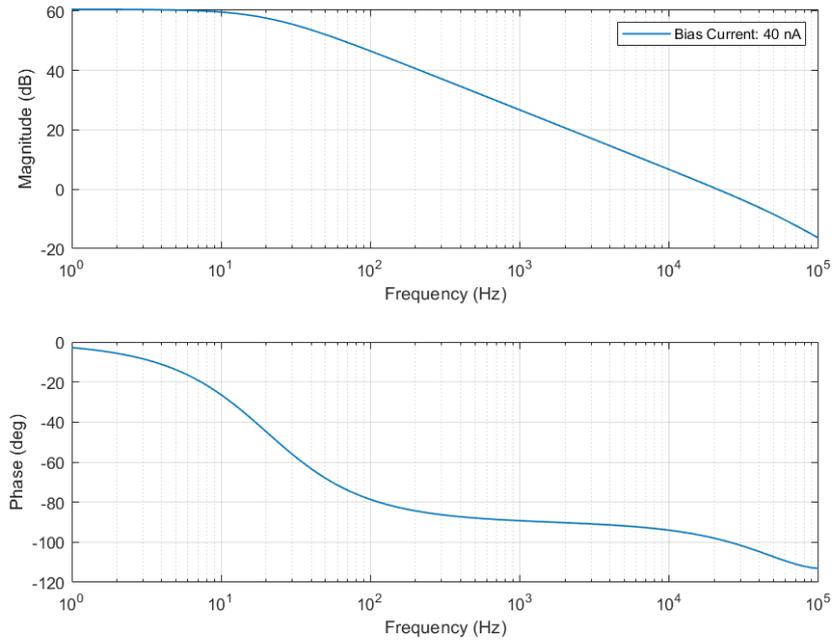


Figure 2.15. The simulated frequency response of the proposed OTA

The noise performance of the OTA for different bias currents is shown in Figure 2.16. The noise spectral density is integrated over the acoustic band (300-5500 Hz) and the corresponding input-referred noises for the bias currents of 40 nA, 60 nA, and 80 nA are calculated as  $141.6 \mu\text{V}_{\text{rms}}$ ,  $121.56 \mu\text{V}_{\text{rms}}$ , and  $110.2 \mu\text{V}_{\text{rms}}$  respectively. As a result of utilizing small transconductance of the bulk in our application, the input-referred noise is expected to be higher compared to the input-referred noise of the gate-driven topology which is the drawback of the proposed structure.

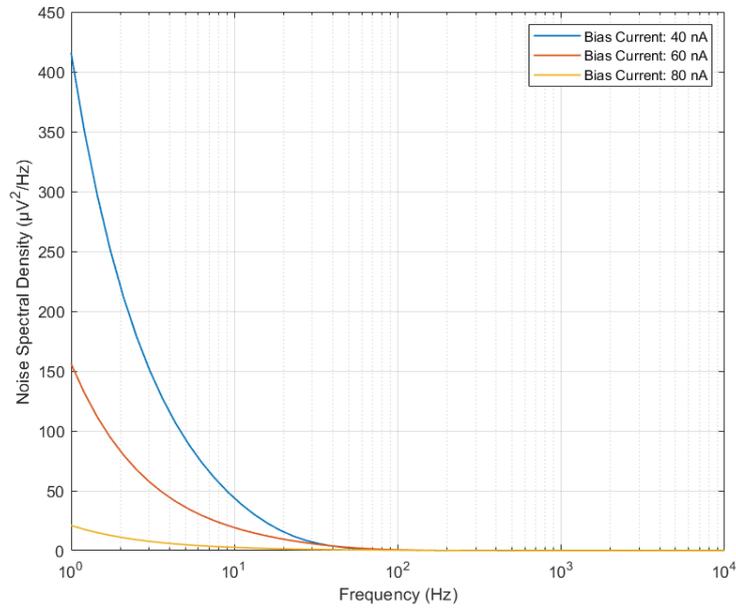


Figure 2.16. The simulated noise spectral density of the proposed OTA

The power consumption of the OTA is presented in Figure 2.17. As expected, the power consumption linearly depends on the bias current. The OTA consumes 3.98 nW at 1 nA bias and the power consumption increases as the bias current increases.

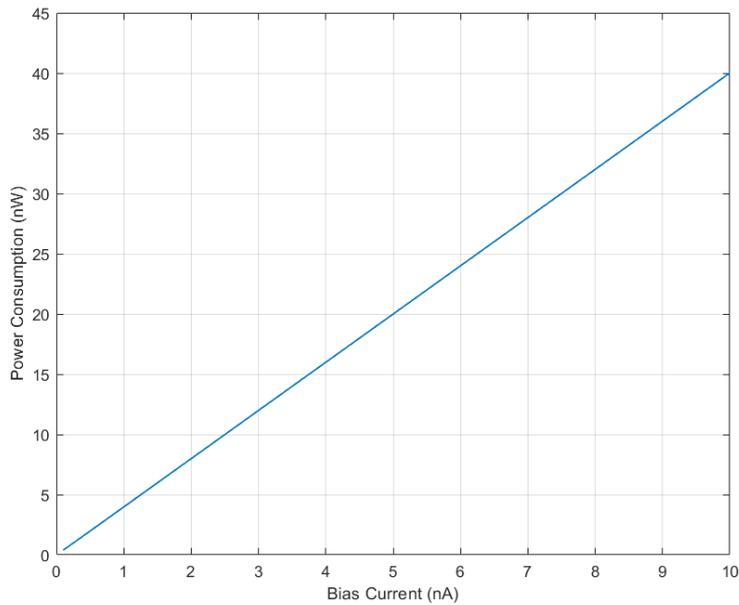


Figure 2.17. The simulated power consumption of the proposed OTA

As the transconductances of the OTA cells in  $G_m$ -C filter topology would determine the filter parameters such as the center frequency band and bandwidth, the controllability of the transconductance through the bias currents is as crucial as the other performance parameters for our application to program the center frequencies and bandwidths of the channels. Figure 2.18 shows that it is possible to tune the transconductance by varying the bias current and these two parameters have a linear relation. In addition, Figure 2.18 proves that the ratio between the bulk and gate transconductance is as calculated in the equations (2.27)-(2.29). This ratio is calculated as 3.25 in the proposed OTA.

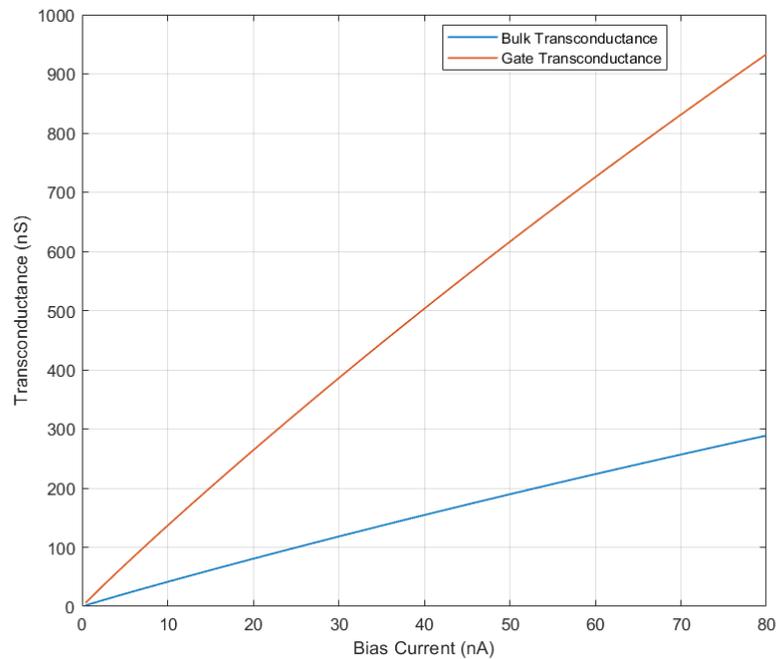


Figure 2.18. The simulated transconductance control of the proposed OTA.

The proposed OTA cell accomplishes the goal of low power consumption by operating all the transistors in the subthreshold region and consumes power not more than 500 nW for the bias currents up to 100 nA. The circuit achieves a small transconductance as desired and the transconductance can easily be controlled through the bias current. Therefore, the proposed OTA is an ideal candidate as an OTA cell in the  $G_m$ -C filter which would be utilized in the speech processor of the fully implantable cochlear implants.

## 2.5.2 Second-order Programmable $G_m$ -C Bandpass Filter

Analog signal processing is preferred to digital signal processing in order to lower the power consumption and miniaturize the speech processor while providing programmability as well as a digital signal processor. To achieve these goals, a highly tunable biquadratic  $G_m$ -C bandpass filter as shown in Figure 2.19 is designed for the acoustic signal processing of the fully implantable cochlear implants.

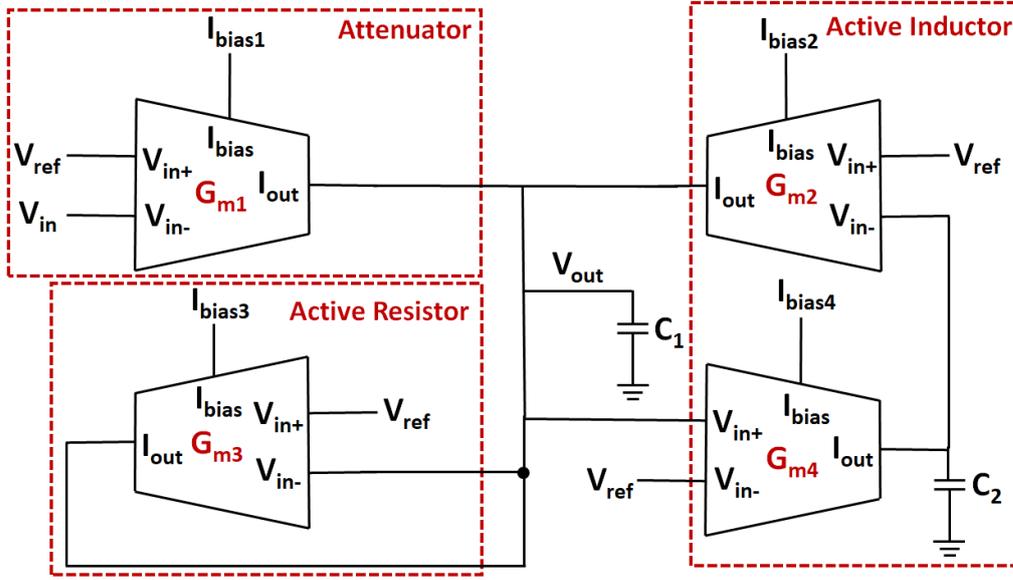


Figure 2.19. The proposed second-order programmable  $G_m$ -C bandpass filter.

The structure consists of an active inductor, an active resistor, and an attenuator formed by four OTA cells and two capacitors, and acts as a resonant RLC filter. The second and the fourth OTA cell with  $C_2$  form an active inductor and determine the resonance frequency of the filter with  $C_1$ . The third OTA cell implements an active resistor and reduces the resonance of the filter. The first OTA cell is an attenuator and compensates for the non-ideal effects on the gain. A reference voltage ( $V_{ref}$ ) of 500 mV is applied to the input terminals to ensure that the bulk-source diode is closed. The transfer function of the filter is defined as follows:

$$H(s) = \frac{\frac{G_{m1}}{C_1} s}{s^2 + \frac{G_{m3}}{C_1} s + \frac{G_{m2} G_{m4}}{C_1 C_2}} \quad (2.32)$$

From equation (2.32), the center frequency, quality factor and gain of the proposed filter can be extracted as follows:

$$\omega_0 = \sqrt{\frac{G_{m2}G_{m4}}{C_1C_2}} \quad (2.33)$$

$$Q = \frac{1}{G_{m3}} \sqrt{\frac{G_{m2}G_{m4}C_1}{C_2}} \quad (2.34)$$

$$H_0 = \frac{G_{m1}}{G_{m3}} \quad (2.35)$$

Equations (2.33)-(2.35) show the programmability options of the proposed filter. The capacitances are determined to be lower than 10 pF not to occupy a larger area on-chip. Based on the equation (2.33), the target frequency band (300-5500 Hz) and intended capacitances (< 10 pF) indicate that the transconductances of OTA cells should be between 10 nS to 350 nS. This range is compatible with the transconductance range of the designed OTA as in Figure 2.18. By varying the transconductances of the second and fourth OTA cell, the resonance frequency of the filter would be determined. Similar to the resonance frequency tuning, the quality factor of the filter would be adjusted by the transconductances of the second, third and fourth OTA cells. The transconductance ratio of the first and third OTA cell control the gain of the filter. In addition to the transconductances, it is possible to program the center frequency and quality factor of the filter through the capacitances.

The proposed filter was designed and simulated in TSMC 0.18  $\mu\text{m}$  CMOS technology. To control the filter parameters, the bias currents of OTA cells are applied externally and the capacitances at the related nodes would be changed from the outside for an additional adjustment. On the other hand, it is possible to control the gain of the filter by varying the reference voltage. Figure 2.20 presents the simulated frequency tunability performance of the proposed filter. The center frequencies are selected such that these are the same as the resonance frequencies of the cantilevers in the multichannel acoustic sensor to compare the frequency responses accurately.

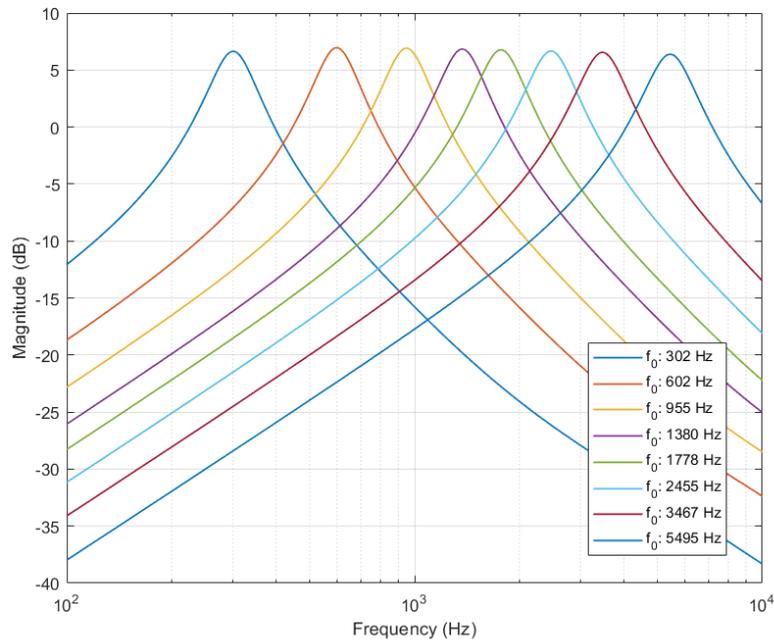


Figure 2.20. The simulated center frequency tunability of the proposed filter

The proposed filter is able to cover any frequency within the target frequency band (300-5500 Hz) by controlling the bias currents to the second and fourth OTA cells. In addition, the bandwidths of the channels are managed to cover the frequency bands between the resonance frequencies which are lost in the mechanical filtering of the acoustic transducer.

The filter also provides the system with quality factor tunability as illustrated in Figure 2.21. It is possible to tune the quality factor of the filter from 1 to 3 by varying the bias current of the third OTA cell so that the frequencies between the resonances would be covered as desired. However, changing the bias current of the third OTA cell affects the gain of the filter. This is the drawback of the filter. The change in the gain would be partially compensated by adjusting the reference voltage. However, the resonance frequency would shift while varying the reference voltage. Therefore, as the gain tunability is not the ideal one, it is determined not to be the priority of the proposed design. Therefore, it is better to tune the gains of the channels in another block.

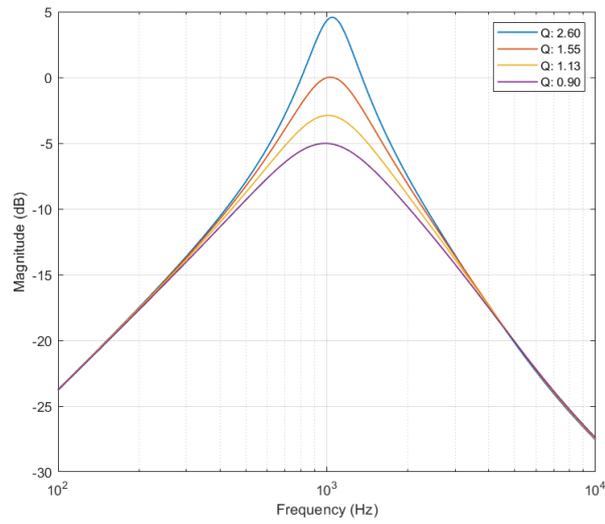


Figure 2.21. The simulated quality factor tunability of the proposed filter.

The noise performance of the filter when the center frequency is set to 950 Hz is given in Figure 2.22. The noise spectral density is integrated over the bandwidth of the channel (600-1520 Hz) and the input-referred noise is calculated as  $179.1 \mu\text{V}_{\text{rms}}$ .

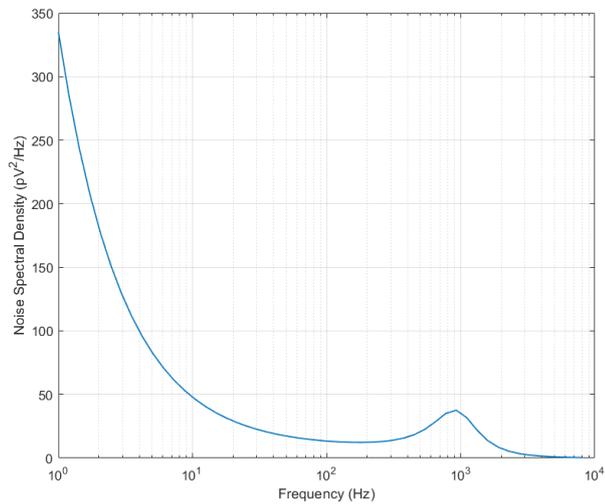


Figure 2.22. The simulated noise spectral density of the proposed filter ( $f_0=950$  Hz).

The linearity performance of the proposed filter is simulated through the 1 dB compression point and it is observed at -8.48 dBm which corresponds to 84.23 mV<sub>rms</sub>. Thus, the dynamic range of the filter is calculated as 53.44 dB.

A sample transient response of the filter is presented in Figure 2.23. In this result, the center frequency of the filter is set to 2300 Hz and five different tones (500, 1000, 2300, 4000, and 6000 Hz) with the same magnitude are applied as input to the filter. As desired, the filter passes the input signal whose frequency is the same as the center frequency of the filter without any compression and suppresses the input signals whose frequencies are different from the center frequency of the filter.

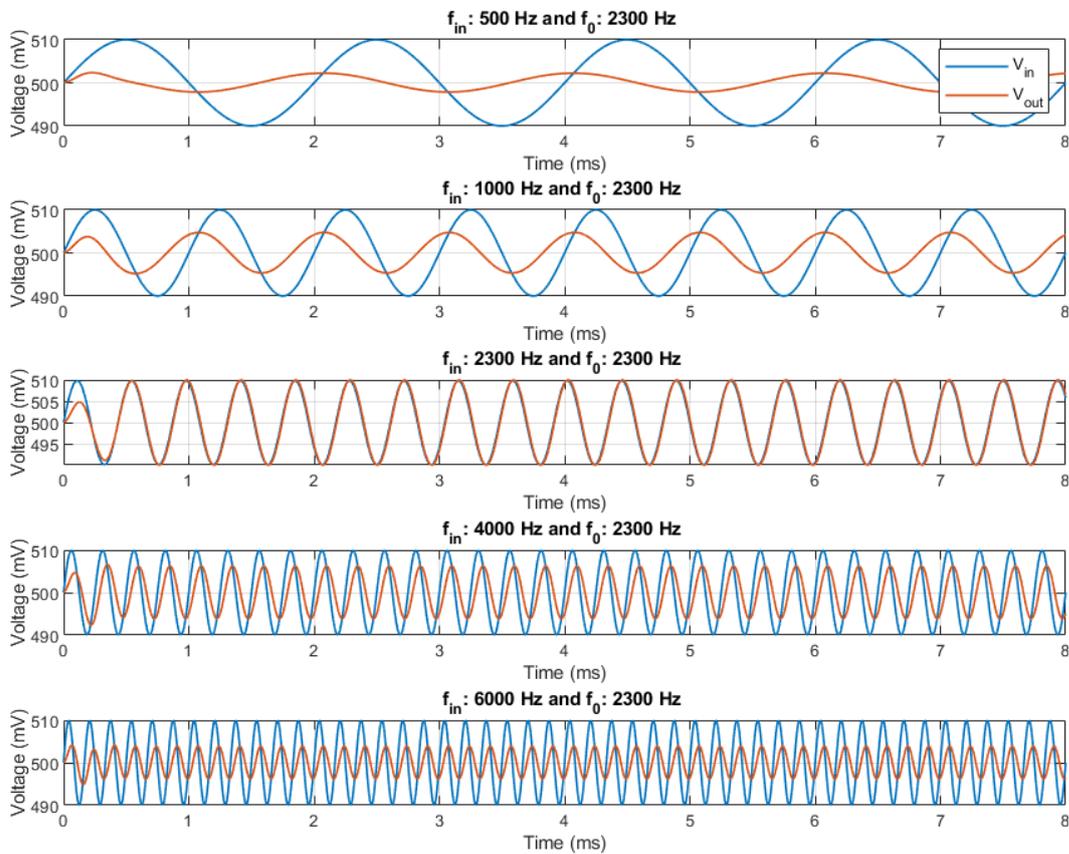


Figure 2.23. The simulated transient analysis of the proposed filter.

The power consumption of the filter depending on the center frequency is depicted in Figure 2.24. To set the center frequency to higher frequencies of the acoustic band, the bias current should be higher. Therefore, as the center frequency of the filter increases, the power consumption of the filter increases as well.

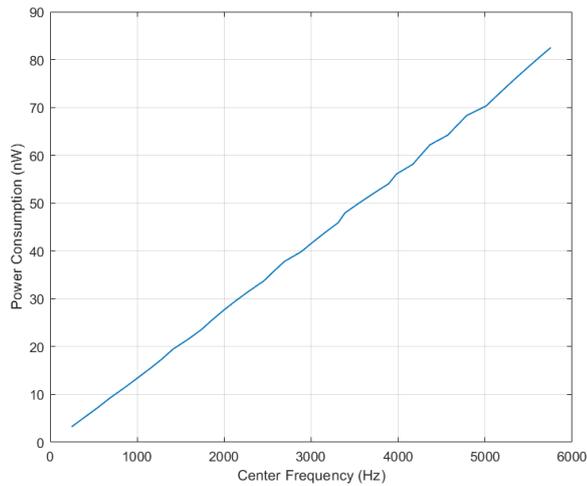


Figure 2.24. The simulated power consumption of the filter depending on the center frequency.

The center frequency of the filter would shift from the value set in the design after the fabrication of the chip due to process variations and the device mismatch. Figure 2.25 illustrates the Monte Carlo simulation result, which the model parameters are randomly varied between specified tolerance limits, for the center frequency over 200 runs. In this result, the center frequency of the filter is set to 950 Hz and an average center frequency of 951 Hz is obtained with a standard deviation of 47 Hz.

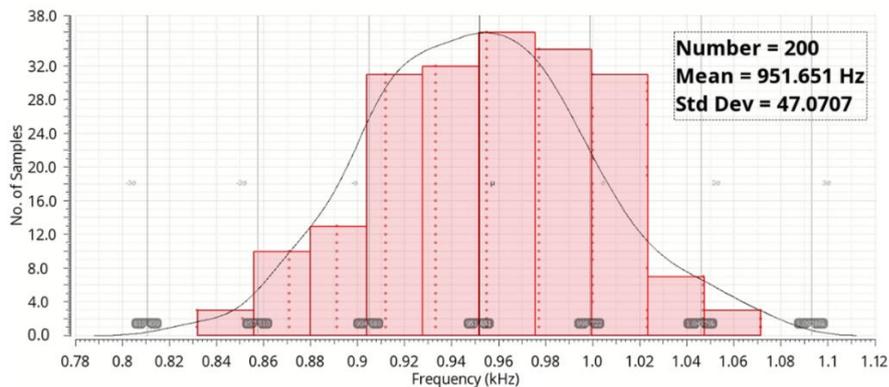


Figure 2.25. The Monte Carlo simulation for the center frequency of the filter ( $f_{\text{center}}=950$  Hz).

## 2.6 Experimental Results

The proposed filter is implemented in TSMC 0.18  $\mu\text{m}$  CMOS High Voltage BCD process. The chip occupies an active area of  $0.085 \text{ mm}^2$  as shown in Figure 2.26 (a). The tests of the chip are performed through a test PCB as illustrated in Figure 2.26 (b). To prevent capacitive loading from the oscilloscope probes, an observation buffer is implemented in addition to the filter. The bias currents to the OTA cells are applied by a source-meter unit in nA range and the capacitance at the output node is adjusted externally to tune the center frequency and quality factor of the filter. The reference voltage is changed to regulate the gain of the filter. The input signals are applied to the filter by a signal generator. The outputs are obtained through an oscilloscope and the voltages/currents at the nodes are sensed by using a source-meter unit. A DC supply provides the filter and the buffer with DC voltages of 1 V and 1.8 V respectively.

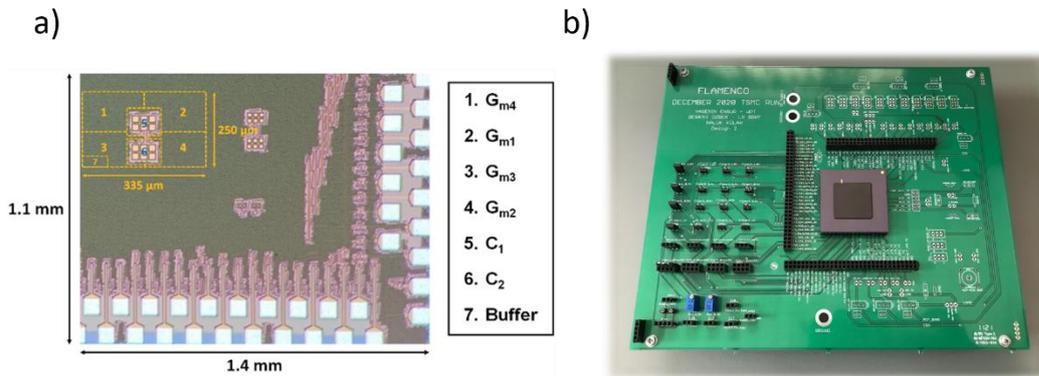


Figure 2.26. a) The micrograph of the implemented filter, b) test PCB of the chip.

The center frequency tunability performance of the filter is demonstrated in Figure 2.27. In this test, the bias currents are selected such that the center frequency of the filter is comparable to the resonance frequencies of the multichannel acoustic transducer and the simulation results of the same bias currents. It is shown that the filter is able to cover the target acoustic band (300-5500 Hz) and the center frequency of the filter can be tuned to any frequency within this band as claimed in the simulation results.

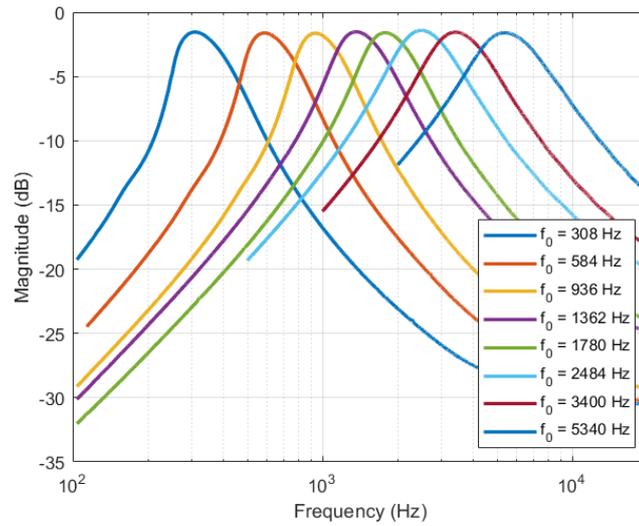


Figure 2.27. The measured center frequency tunability performance of the filter.

The result also proves that the proposed filter has a better performance in terms of the coverage of the acoustic band compared to multichannel acoustic transducer (Figure 1.3). There is no lost bands in between the center frequencies and the system achieves almost ideal auditory filter characteristics (Figure 1.2). For an ideal auditory filter, the bandwidth of each channel should be programmable as well. The filter is able to program the quality factor of the channel as shown in Figure 2.28.

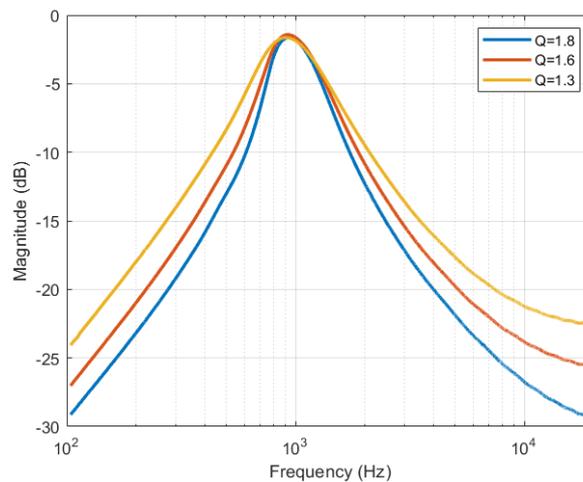


Figure 2.28. The measured quality factor tunability performance of the filter.

In case of unsuccessful insertion of the cochlear electrode, there might be several channels that cannot operate as desired. In addition, due to impedance change over time, the related channel would not effectively stimulate the auditory nerve. In such cases, the results show that the proposed filter is able to cover the lost band by expanding the bandwidths and shifting the center frequencies of the remaining channels such that the hearing at the frequency band of the faulty node would be recovered. The multichannel acoustic transducer cannot realize this operation since it is not possible to change the bandwidths and resonance frequencies of the cantilevers after the fabrication.

Although the tuning of the gain is not the priority of the design, the gain of the filter can be adjusted as presented in Figure 2.29. However, while tuning the gain, the center frequency and quality factor of the channel would shift from the desired values. That is why it is not preferred in this design.

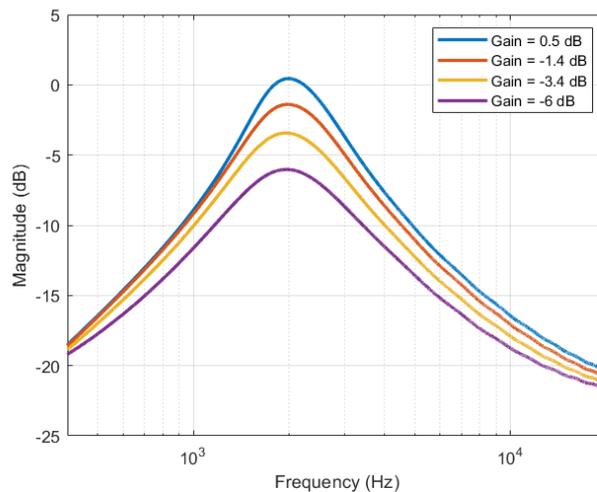


Figure 2.29. The measured gain tunability performance of the filter.

The transient response of the filter is obtained based on the cases given in the simulation results (Figure 2.23) to compare the simulation and the measurement accurately. The input signals with five different frequencies are applied to the filter when the center frequency of the filter is tuned to 2300 Hz. Figure 2.30 illustrates that the measurement results are in agreement with the simulation results in terms of filtering characteristics.

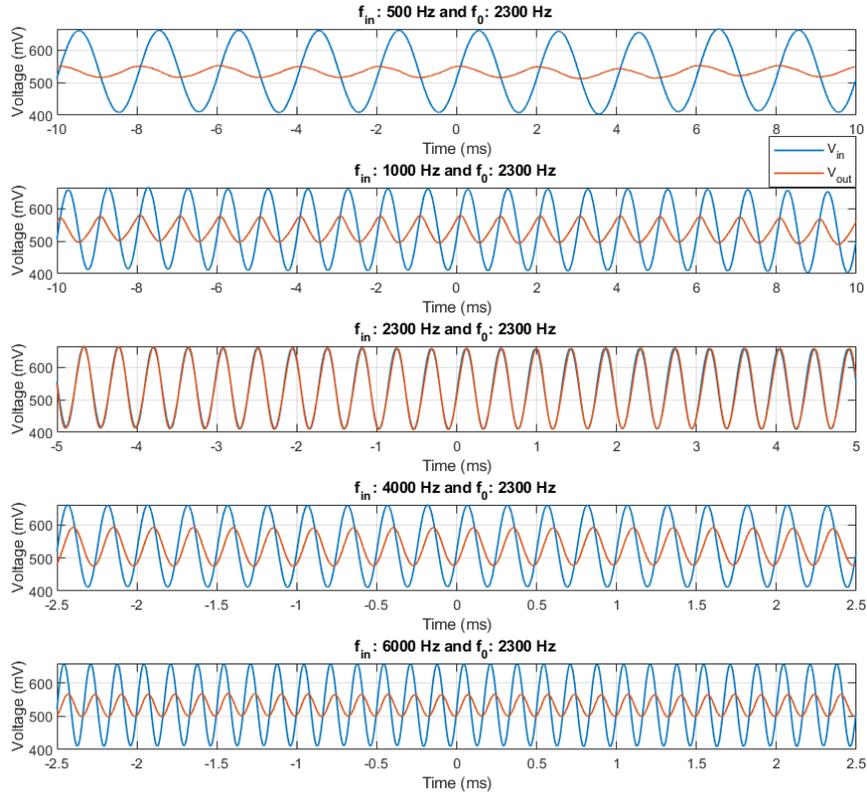


Figure 2.30. The measured transient analysis of the filter.

The in-band linearity performance of the filter is measured when the input signal is sinusoidal at 1000 Hz. 1 dB compression point is observed at -21.7 dBV which equals 82.21 mV<sub>rms</sub> as demonstrated in Figure 2.31. There is a small shift from the simulated value of 84.23 mV<sub>rms</sub>. The input-referred noise of the filter is measured as 207.4  $\mu$ V<sub>rms</sub> when the center frequency is 950 Hz. This noise level is higher compared to the simulation result of 179.1  $\mu$ V<sub>rms</sub>. Thus, the dynamic range is calculated as 51.98 dB which is lower than the simulated dynamic range of 53.44 dB as expected.

The filter consumes 13.2 nW when the filter is biased such that the center frequency of the filter is 950 Hz. To compare the measurement with the expectation correctly, this bias is applied in the simulation such that the power consumption in the simulation is 13.2 nW. The corresponding resonance frequency is observed as 977 Hz. The difference of 27 Hz is in agreement with the Monte Carlo simulation which predicts a standard deviation of 47.07 Hz due to process variations and the device mismatch.

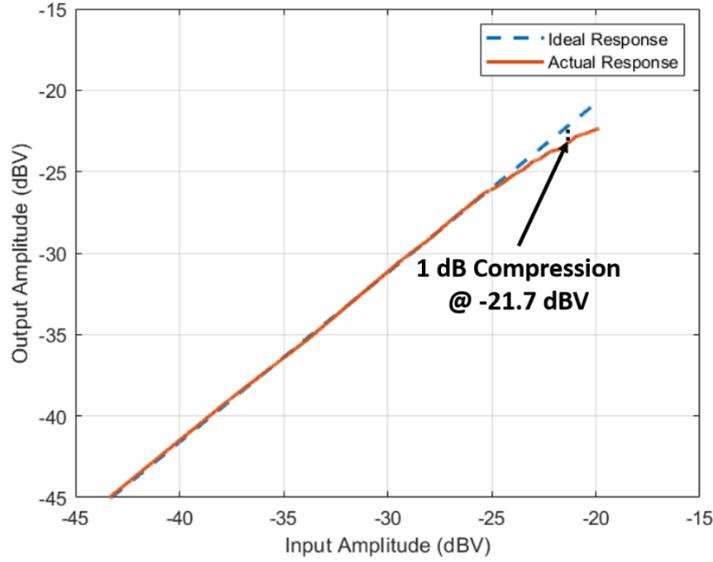


Figure 2.31. The measured linearity performance of the filter.

## 2.7 Summary and Discussion

Table 2.1 compares the performance of the designed filter to the CMOS bandpass filters reported in the literature. The comparison table only considers the works presented with the experimental results and excludes the works with simulation results. The important performance parameters of a CMOS bandpass filter would be the power consumption, dynamic range, and frequency band. Based on these parameters, a Figure-of-Merit would be defined as follows [12]:

$$FoM = \frac{Power \cdot V_{DD}}{N \cdot f_0 \cdot DR} \quad (2.36)$$

where N represents the filter order, DR denotes the dynamic range,  $f_0$  is the center frequency of the filter, and a lower FoM corresponds to a better performance.

The proposed filter is able to cover the frequency band of 100-8000 Hz with a tunable quality factor while consuming power in nW range. The experimental results confirm that the proposed filter achieves a better FoM compared to the highlighted designs as indicated in Table 2.1.

Table 2.1 Performance summary and comparison with state-of-the-art

	[46]	[47]	[48]	[49]	<i>This Work</i>
Technology ( $\mu\text{m}$ )	0.35	0.35	0.35	0.18	0.18
Supply Voltage (V)	1	1	3.3 <sup>1</sup>	1	1
Filter Order	2	6	2	4	2
Frequency Range (Hz)	40-40000	100-25000	20-20000	300-2400	100-8000
Area ( $\text{mm}^2$ )	0.04	0.23	0.13	0.04	0.08
Dynamic Range (dB)	45	49	62.6	52	51.98
Power	2 $\mu\text{W}$ @ 40000 Hz	68 nW @ 670 Hz	192 nW @ 200 Hz	61 nW @ 300 Hz	13.2 nW @ 950 Hz
FoM	$5.56 \times 10^{-13}$	$3.45 \times 10^{-13}$	$253 \times 10^{-13}$	$9.77 \times 10^{-13}$	<b><math>1.33 \times 10^{-13}</math></b>

<sup>1</sup>assumed for a 0.35  $\mu\text{m}$  CMOS process

Referring to the design specifications, the operation of the proposed filter prevails over the operation of the acoustic transducer based on the experimental results. The bandwidths of the channels which are formed by the proposed filter are wide enough to cover the frequency bands in between the center frequencies. However, these frequency bands are lost in the multichannel acoustic transducer due to the high-Q nature of the structure. Furthermore, the center frequencies and bandwidths of the channels can be controlled to maximize hearing for each patient and cover the lost frequency bands due to the faulty channels. However, the center frequencies and the bandwidths of the multichannel acoustic transducer are fixed and not controllable after the fabrication. Thus, replacing the mechanical filtering of the multichannel acoustic transducer with the electrical filtering of the proposed filter would provide the cochlear implant with a better speech processing performance.

Considering the success of the proposed filter, a complete analog front-end that interfaces with the single-channel acoustic sensor for a 12-channel fully implantable cochlear implant system is designed as second-generation.



## CHAPTER 3

### ULTRA LOW-POWER HIGHLY PROGRAMMABLE ANALOG FRONT-END

#### 3.1 Motivation

The main goal of fully implantable cochlear implants is to eliminate the external components of a microphone and speech processor. Therefore, the bulky speech processor should be miniaturized to a small chip that would fit into the middle ear. In addition, this chip should effectively process the sound to provide the patients with a hearing as natural as possible while consuming low power to extend the battery life of the implant and providing programmability for the channels to achieve the best speech perception for each patient.

The experimental results of the proposed filter demonstrate that the filter is able to accomplish the requirements of the low power operation (13.2 nW @950 Hz), high programmability (center frequency and bandwidth), and miniaturization (0.085 mm<sup>2</sup>) and performs better than the mechanical filtering of the multichannel acoustic transducer. Thus, it is convenient to implement the proposed filter to the speech processing block of the fully implantable cochlear implants.

To eliminate the external microphone, an implantable sensor whose dimensions are small enough for the tympanic cavity is required. The size of the multichannel acoustic transducer is not compatible with this volume as presented in Figure 1.1. Therefore, a single-channel piezoelectric acoustic sensor is considered as an alternative to the multichannel acoustic transducer. This sensor would have a resonance frequency far from the acoustic band and operate in the non-resonance region like an accelerometer. As the resonance frequency is at higher frequencies, the length of the cantilever would be small enough to fit into the middle ear so that the sensor would be mounted onto the ossicles.

Combining the single-channel acoustic sensor with the proposed filter and other processing blocks would result in a novel fully implantable cochlear implant system. However, there are several issues to be improved in the first-generation chip in order to achieve the novel fully implantable cochlear implant system.

Firstly, there is only one filter implemented in the first-generation chip. It means that only one frequency component of the incoming sound would be processed at a time. Thus, there should be multiple filters to process the sound as desired in the next design. Secondly, the passband input-referred noise of the previous design is  $207 \mu\text{V}_{\text{rms}}$ . As the single-channel acoustic sensor will operate in the non-resonance region, the output level of the sensor would be very low for the low-levels of SPL. Therefore, the input-referred noise becomes more important since it determines the minimum signal which the circuit can handle. To provide a lower hearing threshold, the input-referred noise of the previous design ( $207 \mu\text{V}_{\text{rms}}$ ) should be improved. Lastly, the resonance frequencies and the bandwidths of the filters are determined through the transconductances of the OTA cells and the transconductances of the OTA cells are determined by the bias currents. In the first design, these bias currents were applied from an external source to OTA cells. Therefore, these currents should be generated internally and controlled digitally in the second-generation chip. To overcome these issues and interface with the single-channel acoustic sensor effectively, a complete analog front-end circuit is designed as the second-generation.

This chapter presents the design of the ultra-low-power highly programmable analog front-end for 12-channel fully implantable cochlear implants. In the proposed analog front-end, a common LNA with very low input-referred noise and high gain amplifies the very low-level outputs of the single-channel acoustic sensor so that the hearing threshold is significantly improved. The output of LNA is divided into twelve channels and each channel includes the proposed filter in the previous design with different center frequencies and bandwidths. Each filter has circuit parameters optimized to the frequency for which the channel is responsible. The outputs of the filters are fed to VGAs in order to control the signal levels at each channel. This allows amplifying desired frequencies in the operation of the cochlear implant.

Section 2 explains the design specifications of the proposed analog front-end circuit. In Section 3, the detailed analysis of the LNA, filterbank, VGAs, current reference, and control block is given. The operation of the analog front-end is demonstrated through the simulation results in Section 4 and the performance of the system is discussed in Section 5.

### **3.2 Design Specifications**

The proposed analog front-end should successfully process the output of the single-channel acoustic sensor and transmit the outputs to the stimulation part. Considering the requirements of the fully implantable cochlear implant systems and foreseeing the operation of the single-channel acoustic sensor, the design specifications are determined as follows:

There are two limitations on the power consumption of the proposed analog front-end. The first one is that the ratio between the power consumption of the proposed analog front-end and the remaining blocks in the speech processing IC with stimulation part should not exceed 5%. The interface electronics of the FLAMENCO project consume around 470  $\mu\text{W}$  [26]. Therefore, the first limit for the power consumption is 23.5  $\mu\text{W}$ . The power consumption of the proposed analog front-end should be comparable to state-of-the-art. Recent studies on the analog front-end of fully implantable cochlear implants [6] and implantable biomedical circuits [50] operate with an average power consumption of 10  $\mu\text{W}$ . As a result, the limit on the power consumption of the proposed analog front-end is determined as 10  $\mu\text{W}$  and would be acceptable up to 23.5  $\mu\text{W}$ .

The sensitivity of the single-channel acoustic sensor and input-referred noise of the proposed analog front-end are two parameters that determine the hearing threshold level of the proposed system. The input-referred noise should be lower than the voltage level which the acoustic sensor is able to provide at threshold SPL. Figure 3.1 shows the relation between SPL and a corresponding acceleration of umbo [21].

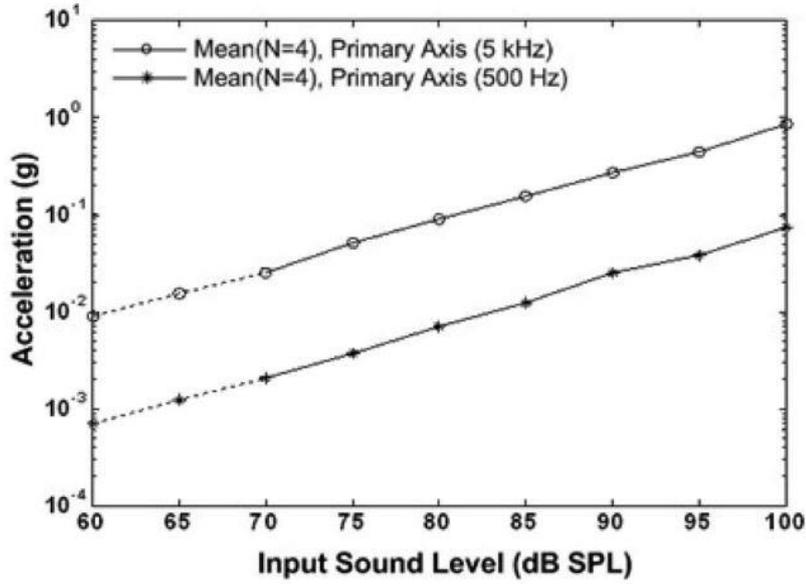


Figure 3.1. The relation between input SPL and acceleration of umbo [21].

According to the result, the acceleration of the umbo is higher in higher frequencies, and the acceleration increases as the input SPL increases. It is determined that the proposed analog front-end should have a hearing threshold of at least 60 dB SPL for all frequencies. This threshold level corresponds to an acceleration level of  $10^{-2}$  g at higher frequencies and  $10^{-3}$  g at lower frequencies. Therefore, the input-referred noise of the proposed analog front-end should be lower than the voltage level which the single-channel acoustic sensor provides at  $10^{-3}$  g input acceleration. Although the design of a single-channel acoustic transducer is not in the scope of this thesis, the sensitivity of the sensor is predicted as  $20 \text{ mV}_{\text{rms}}/\text{g}$  based on the performance of the energy harvester chip of FLAMENCO which would be treated as a single-channel piezoelectric acoustic transducer. Thus, it is determined that the input-referred noises of the proposed analog front-end channels should not exceed  $20 \text{ }\mu\text{V}_{\text{rms}}$ .

Each block in the proposed analog front-end should be programmable. Firstly, the single-channel acoustic sensor would have a dominant noise at the resonance frequency. This noise should be amplified through LNA. Therefore, the bandwidth of LNA should be controllable in order to be compatible with the sensors with different resonance frequencies. Secondly, the center frequency and bandwidth of each channel should be programmable to provide best hearing for each individual

and compensate the loss of frequency bands in case of faulty channels. Lastly, the signal level of each channel should be tunable to amplify specific frequencies before transmitting to the stimulation part.

The programmability of the blocks is provided by the bias currents of the blocks. Therefore, these bias currents should be generated internally and controlled digitally from the outside. The block diagram and signal flow of the proposed analog front-end is illustrated in Figure 3.2.

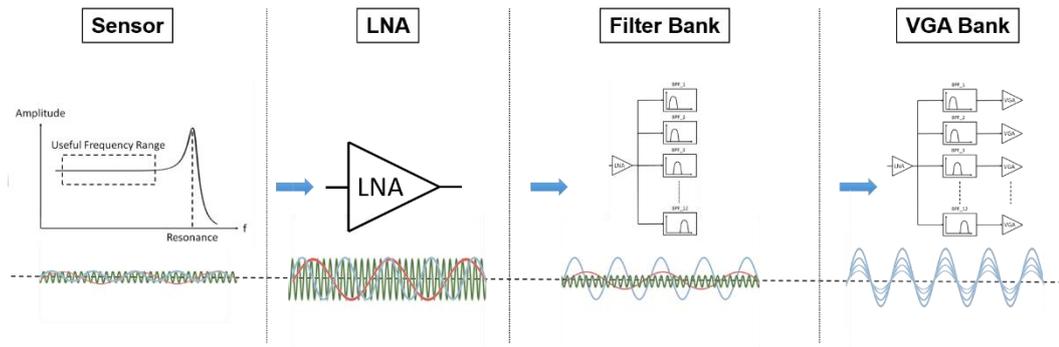


Figure 3.2. The block diagram and signal flow of the proposed analog-front end.

### 3.3 Circuit Design and Analysis

#### 3.3.1 Low Noise Amplifier

The filters in the analog front-end are driven from the bulk and operate in the subthreshold region. Therefore, the operating current is very low which results in a higher noise level ( $207 \mu V_{\text{rms}}$  in first-generation) compared to the noise in the design goal. To decrease the input-referred noise of the system so that the analog front-end is able to process the low-level outputs of the single-channel acoustic sensor, an LNA is designed as the first block of the proposed analog front-end. LNAs usually determine the overall noise performance and dominate the power consumption of the analog front-ends reported in the literature [51]. Thus, it is important to optimize the power and noise trade-off of LNA for an efficient analog front-end.

To improve the trade-off between power and noise, several circuit techniques have been utilized in the literature such as folded cascode with low current folds [52], transconductance boosting via current splitting [53], and stacked current reusing [54]. The logic behind these techniques is to achieve maximum transconductance for a given bias current to the system. As the noise performance of LNA is dominated by the input pair, most of the bias current should be separated for the input pair. As a stacked current reuse amplifier has the lowest reported noise efficiency factor (NEF) (1.01 [54]) compared to the other techniques, a stacked input stage current reuse amplifier is designed for the proposed analog front-end.

The operational principle of the topology would be explained through two stacked input stage version for simplicity as depicted in Figure 3.3 [54]. In this structure, the input voltages are converted to currents through the two stacked differential pairs. The transistors of each stage have a succeeding pair. Therefore, the value of current flows through one branch of the second stage is half of the current flow through one branch of the first stage and thereby a quarter of the bias current. If the aspect ratios of the transistors are set such that the aspect ratios are halved in the next stage and considering the total current in each stage is equal, the transconductance and gate-to-source voltages would be the same as indicated in the following equations:

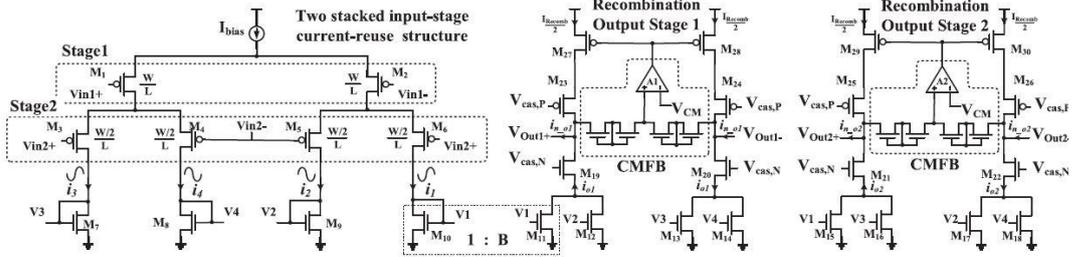


Figure 3.3. The two stacked input stage current reuse amplifier [54].

$$g_m = \sqrt{2\mu C_{ox} \left(\frac{W}{L}\right) I_d} \quad (3.1)$$

$$V_{gs} = V_{th} + \sqrt{\frac{2I_d}{\mu C_{ox} \left(\frac{W}{L}\right)}} \quad (3.2)$$

The small-signal currents in the branches of the last stage ( $i_1$ - $i_4$ ) given in equation (3.3) are mirrored towards the output stage with multiplying factor of B where these currents are recombined to generate differential output voltages ( $V_{out1+}$ ,  $V_{out1-}$ ,  $V_{out2+}$ ,  $V_{out2-}$ ).

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ -1 \\ -1 \end{bmatrix} \cdot \frac{g_{m1}V_1}{4} + \begin{bmatrix} 1 \\ -1 \\ 1 \\ -1 \end{bmatrix} \frac{g_{m2}V_2}{4} \quad (3.3)$$

To stabilize the output common-mode voltage, common-mode feedback should be utilized. In this circuit, the output common-mode voltage is sampled by two resistors whose resistances are very high. To achieve such high resistances without occupying much area on-chip, pseudo resistors are used. The sampled output common voltage is compared to the desired common voltage level by a single-ended differential pair. In the end, the bias voltages for M27-M28 and M29-M30 are generated.

The most important parameter of the block is the input-referred noise. By using the thermal noise density of MOSFET and the multiplying factor of B, the output current noises are calculated as follows:

$$i_{n,o1}^2 = 4KT\gamma(2g_{m1} + 4g_{m7} + 4B^2g_{m11} + 2B^2g_{m27}) \quad (3.4)$$

$$i_{n,o2}^2 = 4KT\gamma(4g_{m3} + 4g_{m7} + 4B^2g_{m15} + 2B^2g_{m29}) \quad (3.5)$$

where K represents Boltzmann constant, T is the temperature in Kelvin and  $\gamma$  is a constant which is 2/3 for long channel devices and 2~3 for short channel devices.

From equations (3.4), (3.5), the input-referred noises are calculated by dividing the output current noises by the gain of the amplifier as follows:

$$V_{n,in1}^2 = \frac{8KT\gamma}{g_{m1}} \left( 1 + \frac{2g_{m7}}{g_{m1}} + \frac{2g_{m11}}{B^2g_{m1}} + \frac{g_{m27}}{B^2g_{m1}} \right) \quad (3.6)$$

$$V_{n,in2}^2 = \frac{8KT\gamma}{2g_{m3}} \left( 1 + \frac{2g_{m7}}{2g_{m3}} + \frac{2g_{m15}}{2B^2g_{m3}} + \frac{g_{m29}}{2B^2g_{m3}} \right) \quad (3.7)$$

Equations (3.6), (3.7) show that a lower input-referred noise is achieved for lower B.

Increasing the number of stacked input stages would improve the noise efficiency factor [54]. However, for n-stage stacked inputs, there are  $2^n$  output currents to be recombined. This exponential relation makes the structure occupy a larger on-chip area for higher n values. Therefore, a four stacked input stage current reuse amplifier is designed for the proposed analog front-end as presented in Figure 3.5.

In this structure, there are 16 currents to be recombined to provide output voltages. The input stages contain very large transistors to decrease flicker noise and the aspect ratios are halved in the next stage. The common-mode feedback circuit sets the output DC level as 500 mV to keep the bulk-source junction diodes of the bulk-driven input pairs in the filters off. To sample the output common-mode voltage, there are two very high-value resistors ( $\sim 1$  Tohm) that are implemented with pseudo-resistors. The pseudo-resistors have very large resistances implemented by two off-state transistors. There are several configurations to implement a pseudo-resistor as shown in Figure 3.4. Since it is not needed to tune the resistance in our application, the configuration indicated in Figure 3.4(a) is utilized in the proposed LNA. This configuration contains two diode-connected PMOS transistors. The corresponding conductance when  $V_{ab} > 0$  and  $V_{SD1,2} < V_{T0}$  would be calculated as follows [55]:

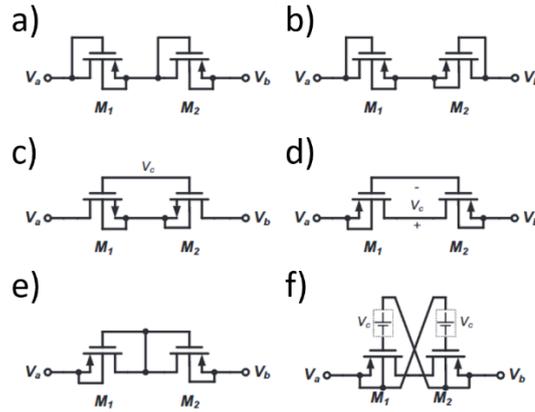


Figure 3.4. The pseudo-resistor structures reported in the literature [55].

$$g_{SD1,2} = \frac{I_S}{nV_T} e^{-\frac{V_{T0}}{nV_T}} [e^{\frac{V_{SD}}{nV_T}} - (1-n)e^{(1-n)\frac{V_{SD}}{nV_T}}] \quad (3.8)$$

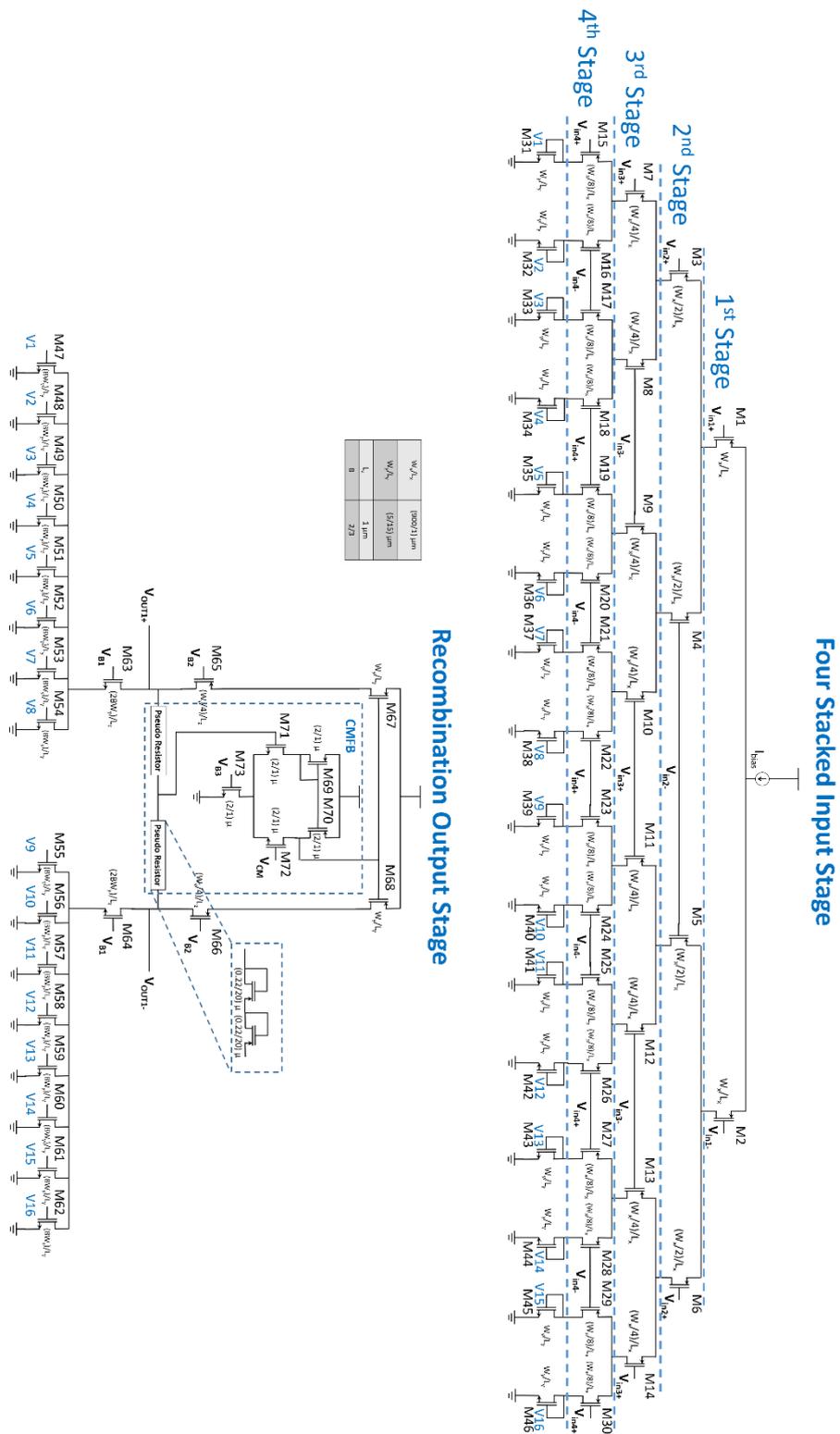


Figure 3.5. The proposed four stacked input stage current reuse amplifier.

To achieve an accurate amplification ratio, the amplifier is implemented with capacitive feedback as depicted in Figure 3.6. In this configuration, the gain of the amplifier is determined by the ratio of  $C_s/C_f$ . A low-frequency pole is added at  $s=1/RC_f$ . The value of R should be very high to minimize the low-frequency cut-off. Therefore, the pseudoresistors are implemented in this configuration as well.

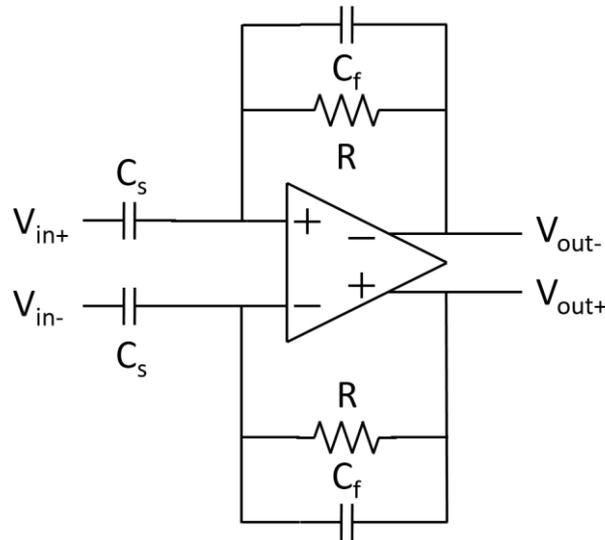


Figure 3.6. The single stage with capacitive feedback.

For our application, the high-frequency cut-off of LNA should be between 8 and 10 kHz depending on the resonance frequency of the single-channel acoustic sensor and the low-frequency cut-off should be as small as possible to reduce  $1/f$  noise of the following stages. The gain of the proposed LNA should be higher than 30 dB to amplify the low-level output of the sensor. Therefore, the parameters to satisfy these conditions are determined as follows:  $C_s/C_f$ : 400, R: 2 Tohms,  $I_{bias}$ : 800 nA, and  $V_{supply}$ : 1.8 V. These parameters would be rearranged based on the top-level simulation of the proposed analog front-end.

The LNA was designed and simulated in TSMC 0.18  $\mu\text{m}$  CMOS technology. The simulated frequency response of the proposed LNA with the mentioned parameters is demonstrated in Figure 3.7. From the result, the low-frequency and high-frequency cut-offs are obtained as 524 mHz and 7.5 kHz respectively which results in a bandwidth of 7.5 kHz. The gain of the LNA is observed as 44.3 dB.

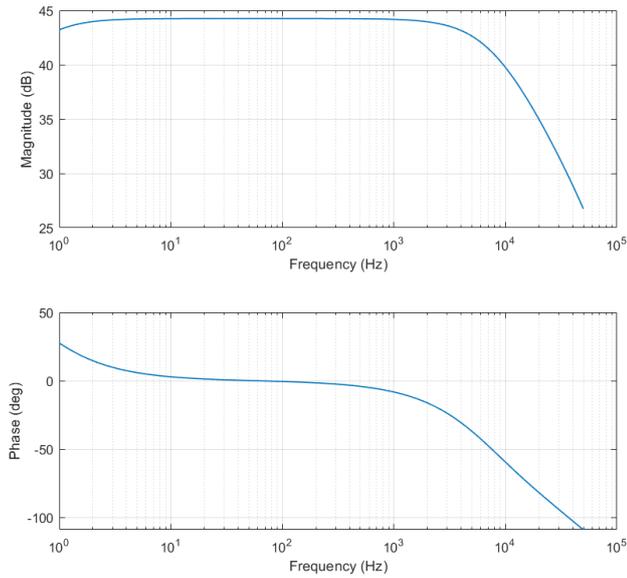


Figure 3.7. The simulated frequency response of the proposed LNA.

The bandwidth or high-frequency cut-off of the LNA would be changed through the bias current while the low-frequency cut-off would be adjusted through the resistance (R) as depicted in Figure 3.8.

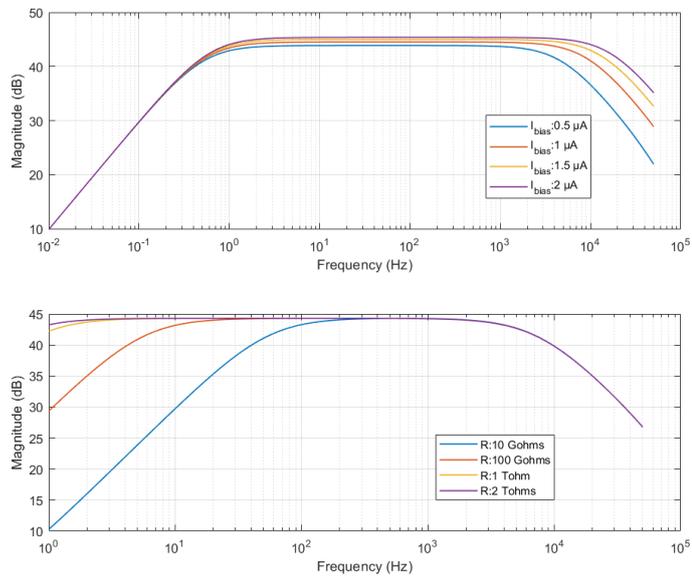


Figure 3.8. The simulated tuning of low and high-frequency cut-offs.

Applying a higher bias current would increase the bandwidth of the LNA. However, the bandwidth is limited in our application based on the resonance frequency of the single-channel acoustic sensor not to amplify the resonance noise. On the other hand, it is desired to minimize low-frequency cut-off so that  $1/f$  noises of the following blocks would be reduced. Therefore, the resistance in Figure 3.6 should be very high as the result indicates. To achieve such a high value of resistance without occupying a very large on-chip area, a pseudoresistor whose resistance is almost 1 Tohm is designed as shown in Figure 3.9.

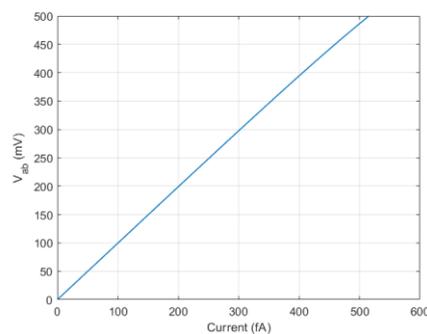


Figure 3.9. The simulated V-I relation of the proposed pseudoresistor.

The gain of the LNA would be altered through the capacitance of  $C_s$  and  $C_f$ . While keeping  $C_f$  constant as 100 fA, the simulated gain tuning by varying  $C_f$  is illustrated in Figure 3.10.

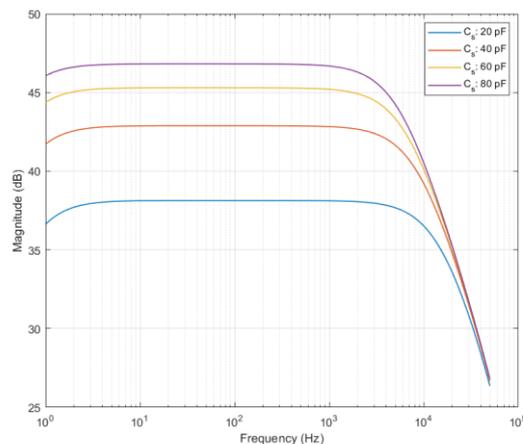


Figure 3.10. The simulated gain tuning of the proposed LNA

The noise performance of the proposed LNA is shown in Figure 3.11. The noise spectral density is integrated over the acoustic band (85-6500 Hz) and the input-referred noise is calculated as  $6.14 \mu\text{V}_{\text{rms}}$ . The total harmonic distortion is observed as less than %1 at  $1.92 \text{ mV}_{\text{pp}}$  in the simulation results.

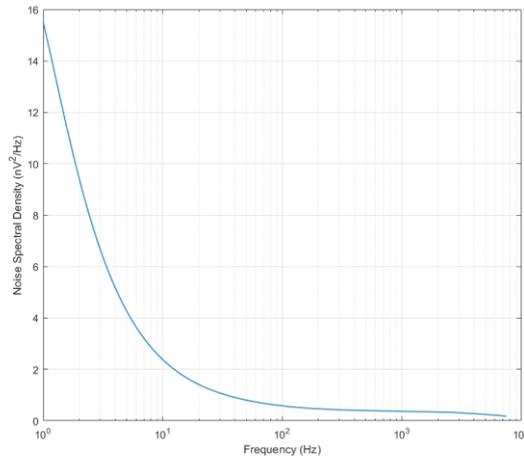


Figure 3.11. The simulated noise spectral density of the proposed LNA.

The proposed LNA consumes  $2.34 \mu\text{W}$  for the bias current of  $800 \text{ nA}$ . The power consumption of the proposed LNA for different bias currents is depicted in Figure 3.12.

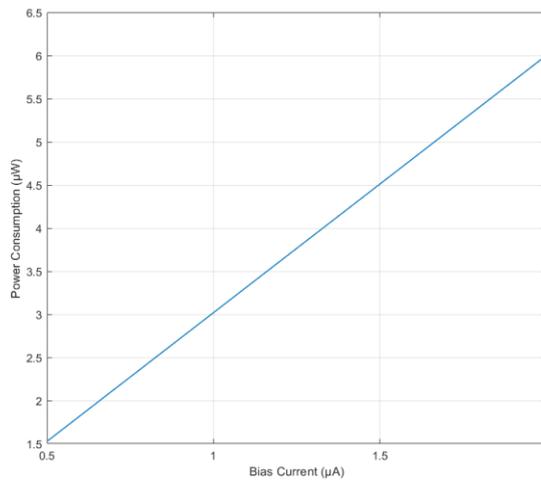


Figure 3.12. The simulated power consumption of the proposed LNA.

### 3.3.2 Filterbank

The performance of the filter in the previous design demonstrated that the proposed second-order  $G_m$ -C bandpass filter topology with bulk-driven subthreshold folded cascode OTA cell was able to achieve the characteristics of an ideal auditory filter with high programmability and low power consumption. However, the first-generation design contains only one filter which makes the processing of only one frequency component possible. Therefore, a filterbank formed by 12 bandpass filters is implemented in the proposed analog front-end to process all of the predefined frequency components simultaneously. Considering the success of the previous design, the same structure is implemented with slight modifications in the OTA cell for the filterbank of the proposed analog front-end as shown in Figure 3.13.

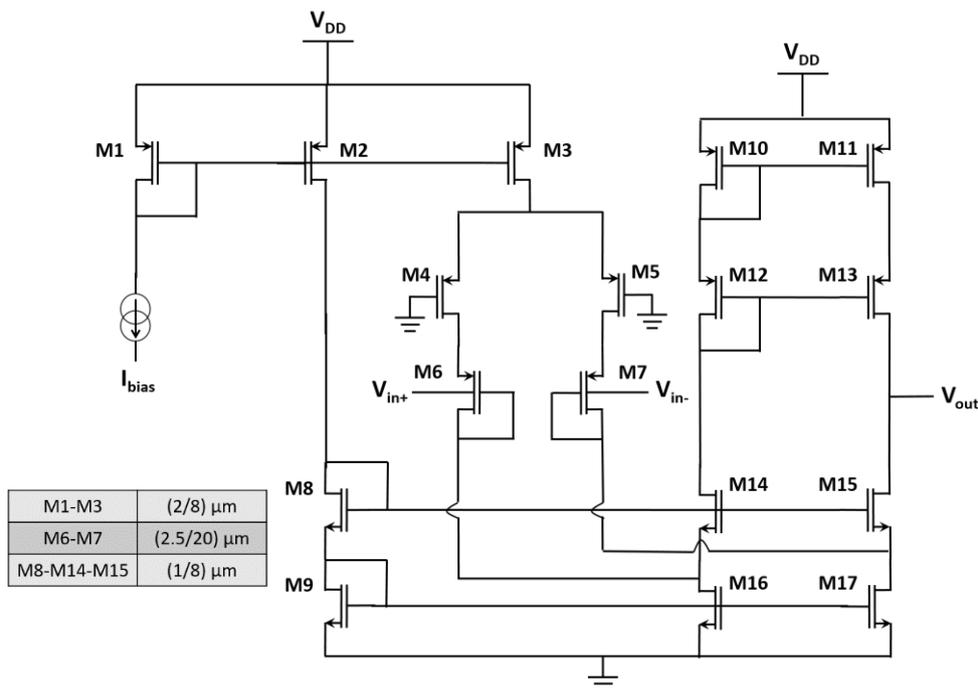


Figure 3.13. The proposed OTA cell for the filterbank of the proposed analog front-end.

Although the intended center frequencies were achieved thanks to the reduction in the transconductance through bulk-driving, it is hard to shift the center frequency in small steps due to a very low-level of bias current. The filters in the filterbank of the

proposed analog front-end should be programmable such that the center frequencies would be shifted in very small steps (e.g. from 335 Hz to 400 Hz) for the patient fitting. Therefore, to overcome this problem, the transconductance should be further reduced so that higher bias currents are applied in exchange for power consumption. In the modified version of OTA, two additional techniques are implemented to further reduce the transconductance in addition to the bulk-driving: source-degeneration and gate degeneration [56]. The transistors of M4 and M5 operate in the deep triode region where the drain-to-source voltages are much smaller than the overdrive voltage ( $V_{sg}-V_{th}$ ). Therefore, there is a linear relationship between the  $V_{ds}$  and  $I_{ds}$  and the transistors act as voltage-controlled resistors. This resistive behavior is utilized to convert the current flowing through the transistors into the voltages through the resistors and these voltages are fed to the sources of the input transistors to decrease the currents. The gate degeneration, on the other hand, converts the currents flowing through the input pair of M6 and M7 into the voltages through the diodes and these voltages are fed back to the gates of M6 and M7 to decrease the currents. The reduction in the bulk transconductance is demonstrated in Figure 3.14.

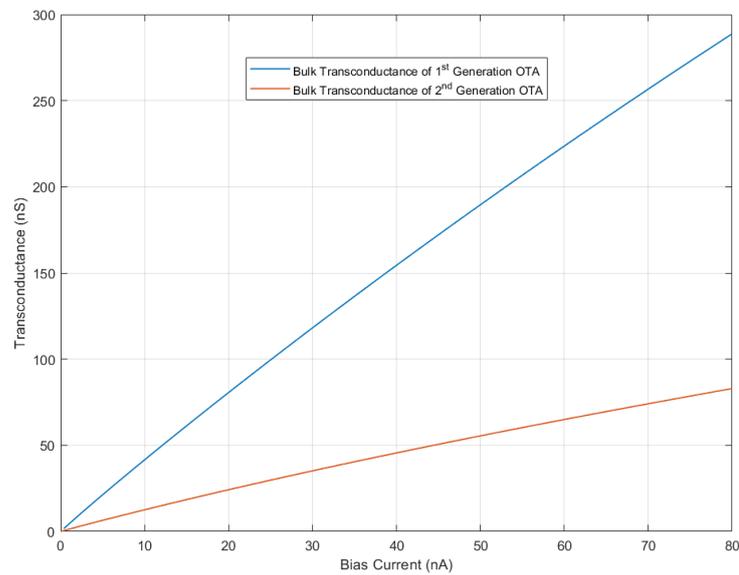


Figure 3.14. The simulated bulk transconductance comparison of 1<sup>st</sup> and 2<sup>nd</sup> generation OTAs

Based on the experimental speech perception scores reported in [57], the center frequencies and bandwidths of the channels are determined as in Table 3.1. In this distribution, the acoustic band of 85-6592 Hz is covered with 12 channels. Each channel has a specific bandwidth and the quality factor of the channel increases as the channel number increases. The same filter topology as in Figure 2.19 is utilized to form 12 bandpass filters in the filter bank. The simulated frequency responses of the channels are demonstrated in Figure 3.15 and achieved center frequencies and quality factors are summarized in Table 3.2.

Table 3.1 The proposed center frequency and bandwidth allocations

	<i>Ch1</i>	<i>Ch2</i>	<i>Ch3</i>	<i>Ch4</i>	<i>Ch5</i>	<i>Ch6</i>	<i>Ch7</i>	<i>Ch8</i>	<i>Ch9</i>	<i>Ch10</i>	<i>Ch11</i>	<i>Ch12</i>
Low-frequency Cut-off (Hz)	85	165	268	402	577	806	1108	1505	2031	2732	3667	4919
Center Frequency (Hz)	125	216	335	490	692	957	1306	1768	2381	3199	4293	5756
High-frequency Cut-off (Hz)	165	268	402	577	806	1108	1505	2031	2732	3667	4919	6592
Quality Factor	1.56	2.1	2.5	2.8	3.02	3.18	3.29	3.36	3.4	3.42	3.43	3.44

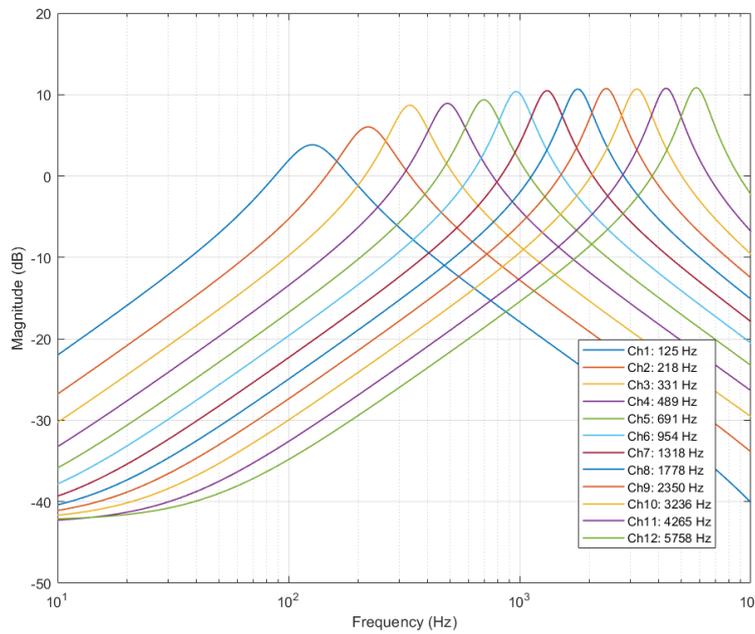


Figure 3.15. The simulated frequency response of the proposed filterbank.

Table 3.2 The achieved center frequency and bandwidth allocations in simulation

	<i>Ch1</i>	<i>Ch2</i>	<i>Ch3</i>	<i>Ch4</i>	<i>Ch5</i>	<i>Ch6</i>	<i>Ch7</i>	<i>Ch8</i>	<i>Ch9</i>	<i>Ch10</i>	<i>Ch11</i>	<i>Ch12</i>
Center Frequency (Hz)	125	218	331	489	691	954	1318	1778	2350	3236	4265	5758
Quality Factor	1.56	1.99	2.70	2.83	2.92	3.28	3.38	3.44	3.45	3.52	3.67	3.69

All of the filters in the filter bank are formed by using the same OTA structure (Figure 3.13). However, each channel has its own characteristics in terms of center frequency and bandwidth. Changing the bias currents to the filters alone would not result in desired characteristics in terms of power consumption, tunability performance, and subthreshold operation. Therefore, to design channel-specific filters with the safe subthreshold operation ( $V_{ds} > 100$  mV), several parameters should be adjusted based on the expectations of the related channel. These parameters are as follows:  $C1=C2=C$  of the bandpass filters,  $I_{bias1}=I_{bias2}=I_{bias4}$  and  $I_{bias3}$ , the aspect ratios of M10-M13, M4-M5, M9, and M16-M17. The parameters that provide the channels with reasonable power consumption and tunability performance are given in Table 3.3.

Table 3.3 The circuit parameters for the proposed filter bank.

	<i>Ch1</i>	<i>Ch2</i>	<i>Ch3</i>	<i>Ch4</i>	<i>Ch5</i>	<i>Ch6</i>	<i>Ch7</i>	<i>Ch8</i>	<i>Ch9</i>	<i>Ch10</i>	<i>Ch11</i>	<i>Ch12</i>
C (pF)	9	9	8	7	6	5	4	4	3	2	1	1
M10-M13 W/L ( $\mu\text{m}$ )	8/8	8/8	8/8	12/8	16/8	20/8	24/8	32/8	32/8	32/8	32/8	32/8
M4-M5 W/L ( $\mu\text{m}$ )	2/8	2/8	12/8	12/8	12/8	12/8	12/8	12/8	12/8	12/8	12/8	12/8
M9, M16, M17 W/L ( $\mu\text{m}$ )	4/8	12/8	22/8	24/8	24/8	24/8	24/8	32/8	32/8	32/8	32/8	32/8
$I_{bias1}=I_{bias2}=I_{bias4}$ (nA)	4	7.3	10	13	16.3	19.1	21.2	30	30.3	28	20	28
$I_{bias3}$ (nA)	2.5	3.5	3.5	4.5	5.5	6	7	10	11	12	12	16.5

As a result of varying parameters, the gain of each channel is different from each other. This would be compensated by the VGA of each channel. The power consumptions and passband input-referred noises are given in Table 3.4.

Table 3.4. The simulated power consumptions and noise performances of the channels.

	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12
Power												
Consumption (nW)	58.1	102.2	134.3	174.3	218.2	253.8	282.1	400	408	384	288.2	402
Input-Referred Noise ( $\mu V_{rms}$ )	159.3	134.2	127.5	129.3	134.1	143.2	157.4	158.6	182.3	221	307.8	309.1

The transconductance of the OTA cell is reduced to provide more precise programmability. To cover the target frequency band with the reduced transconductance, the bias currents to the OTA cells are increased. Therefore, the power consumption of the filters are increased compared to the first design.

To optimize the performance of the filterbank for each patient, the center frequencies and bandwidths of the channels should be programmable. The programmability performance of the filter is demonstrated through channel 6 as shown in Figure 3.16 and Figure 3.17. The gain variations in the results would be compensated by VGAs.

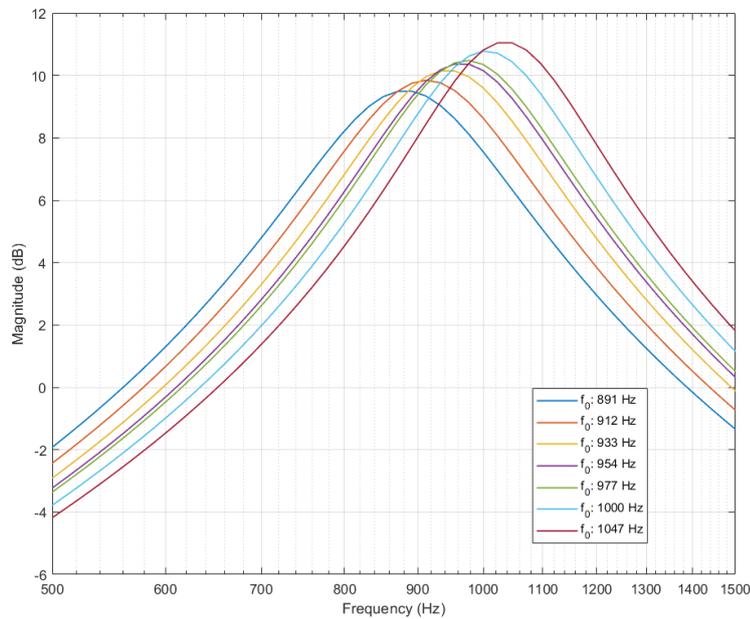


Figure 3.16. The simulated center frequency tunability of 6<sup>th</sup> channel.

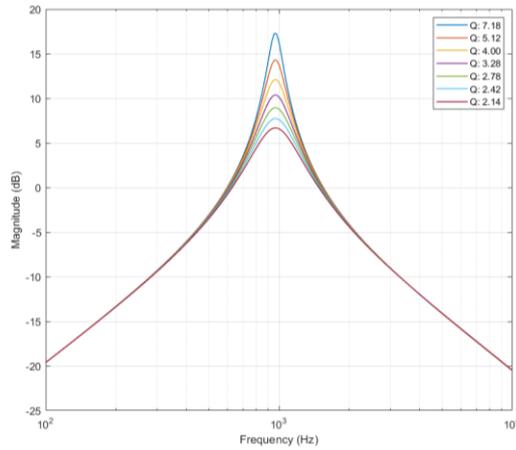


Figure 3.17. The simulated quality factor tunability of 6<sup>th</sup> channel.

To observe the transient response of the filterbank, a sinusoidal input with amplitude of 20 mV<sub>pp</sub>, DC: 500 mV, and f: 954 Hz is applied to the filterbank. Figure 3.18 demonstrates the transient response of the filterbank. The input is amplified in channel 6 and its neighbor channels as the input frequency is the same as the center frequency of channel 6 and suppressed in other channels as desired.

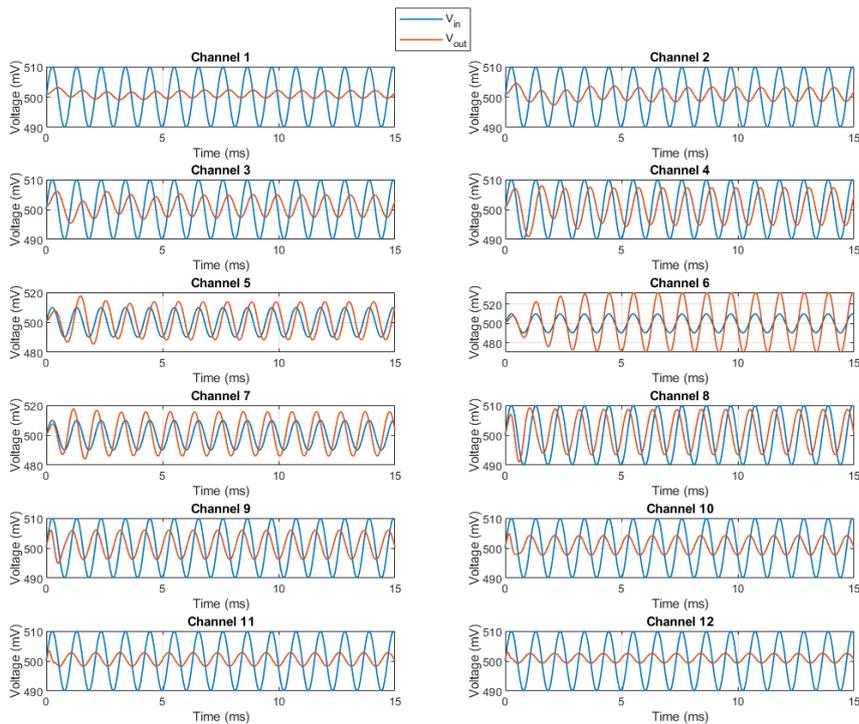


Figure 3.18. The simulated transient response of the filterbank.

### 3.3.3 Variable Gain Amplifier

The signal amplitudes of the channels would be different from each other due to the varying parameters of the filters. Although it is possible to tune the gain in the filter, the center frequency and the bandwidth of the channel would be affected while tuning the gain through the filter. In addition, the signal level of each channel should be reconfigurable to amplify desired frequency bands. Therefore, an additional stage formed by variable gain amplifiers is implemented to have control on the signal levels of the channels.

Since the noise of this stage would be negligible due to the gains of the preceding stages, the important parameters for this block are determined as controllability, power consumption, chip size, and linearity. Thus, the transconductance-ratoned VGA would be suitable structure as the gain can be controlled by the ratio of the input and load transconductance. In addition, this topology can achieve low power operation while occupying a small on-chip area. However, the load stage would introduce distortion and reduce the linearity of the VGA [58]. The proposed VGA and OTA cell are illustrated in Figure 3.19 [59]. The structure is based on  $G_m$ -C integrator and there are two OTAs whose transconductances are controlled by the bias currents. The transfer function in equation (3.9) indicates that the gain can be controlled by varying the transconductances and thereby the bias currents of the OTA cells [36]. As the output DC level of the filters is 500 mV, a reference voltage of 500 mV is applied to the related terminals. All of the transistors operate in the subthreshold region.

$$\frac{V_o}{V_{in}} = \frac{g_{m1}}{sC + g_{m2}} \quad (3.9)$$

The drawback of the structure, lack of linearity, would be improved by employing the degeneration transistors of M3 and M4. To show the improvement in the linearity, two simple differential pairs with and without the degeneration transistors and biased in saturation would be considered as shown in Figure 3.20 [58].

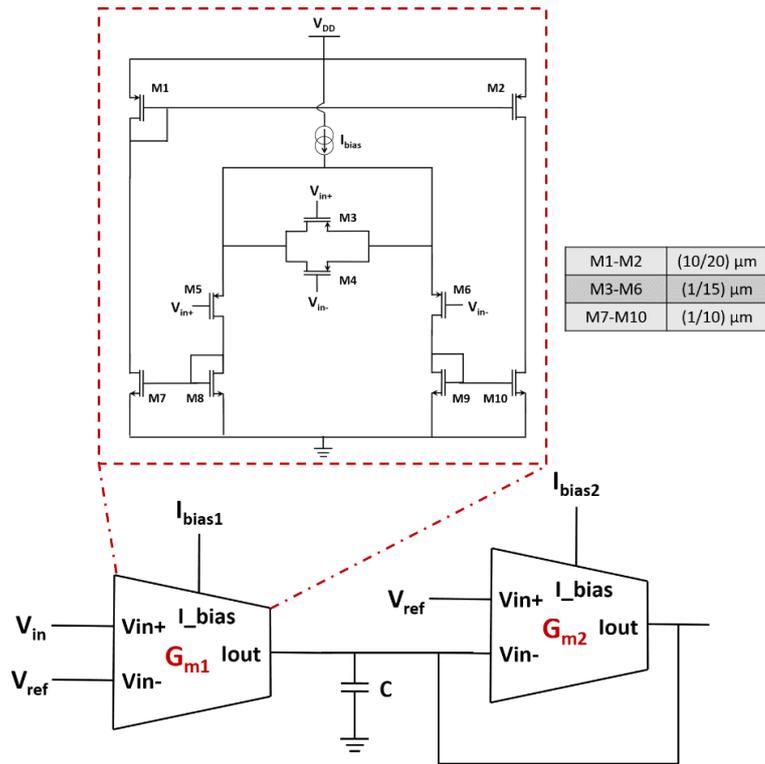


Figure 3.19. The proposed variable gain amplifier [59].

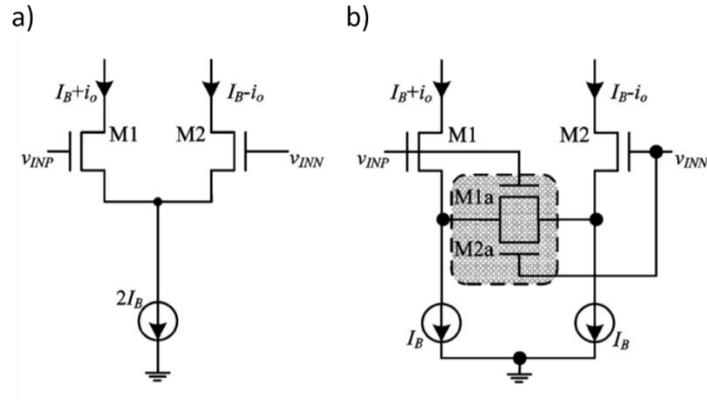


Figure 3.20. a) Differential pair without source degeneration, b) differential pair with source degeneration [58].

The drain current of the differential pair operating in saturation region, neglecting the early effect, is given as follows:

$$i_D = \frac{1}{2}K(v_{GS} - V_{TH})^2, \quad K = \mu C_{ox} \left(\frac{W}{L}\right) \quad (3.10)$$

Taylor series of the differential input voltage would be utilized to express the output current. The output voltage and Taylor series coefficients of the differential pair without degeneration up to the third order are given as follows [60]:

$$i_o = a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 \quad (3.11)$$

$$a_1 = 0.5g_{m1}, \quad a_2 = 0, \quad a_3 = \frac{-K_1^2}{16g_{m1}} \quad (3.12)$$

These coefficients are modified for the differential pair with source degeneration as follows [58]:

$$a_1 = \frac{1}{\alpha} 0.5g_{m1}, \quad a_2 = 0, \quad a_3 = \frac{1}{\alpha^3} \frac{-K_1^2}{16g_{m1}} \quad (3.13)$$

where  $\alpha = 1 + K_1/4K_{1a}$ .

By using the Taylor series coefficients, the third harmonic distortion (HD3) and input-referred 1 dB compression point are given as:

$$HD3 = \frac{1a_3}{4a_1} A_{in}^2 \quad (3.14)$$

$$A_{in,1dB} = \sqrt{0.145 \left| \frac{a_1}{a_3} \right|} \quad (3.15)$$

where  $A_{in}$  is the amplitude.

As the equations (3.14) and (3.15) indicate, the third harmonic distortion is reduced by a factor of  $\alpha^2$  and the input-referred 1 dB compression point is improved by a factor of  $\alpha$  in the case of differential pair with degeneration [60]. Therefore, the transistors of M3 and M4 are integrated to the proposed design to achieve better linearity. The aspect ratios of the input pair and degeneration transistors that provide the best linearity would be found by inserting the Taylor series coefficient into the equation (3.15) (or (3.14)) as given below:

$$A_{in,1dB} = 1,07 \left( \frac{1}{K_5} + \frac{1}{4K_3} \right) = 1,07 \left( \frac{1}{\mu C_{ox} \left( \frac{W}{L} \right)_5} + \frac{1}{4\mu C_{ox} \left( \frac{W}{L} \right)_3} \right) \quad (3.16)$$

Equation (3.16) shows that the aspect ratios should be as small as possible to achieve the best linearity while keeping the transistors in the subthreshold region.

To observe the theoretical expectation above, the lengths of the input pair and degeneration transistors are swept while keeping the widths constant at 1  $\mu\text{m}$ . The linearity performance is simulated through the total harmonic distortion and the result is demonstrated in Figure 3.21.

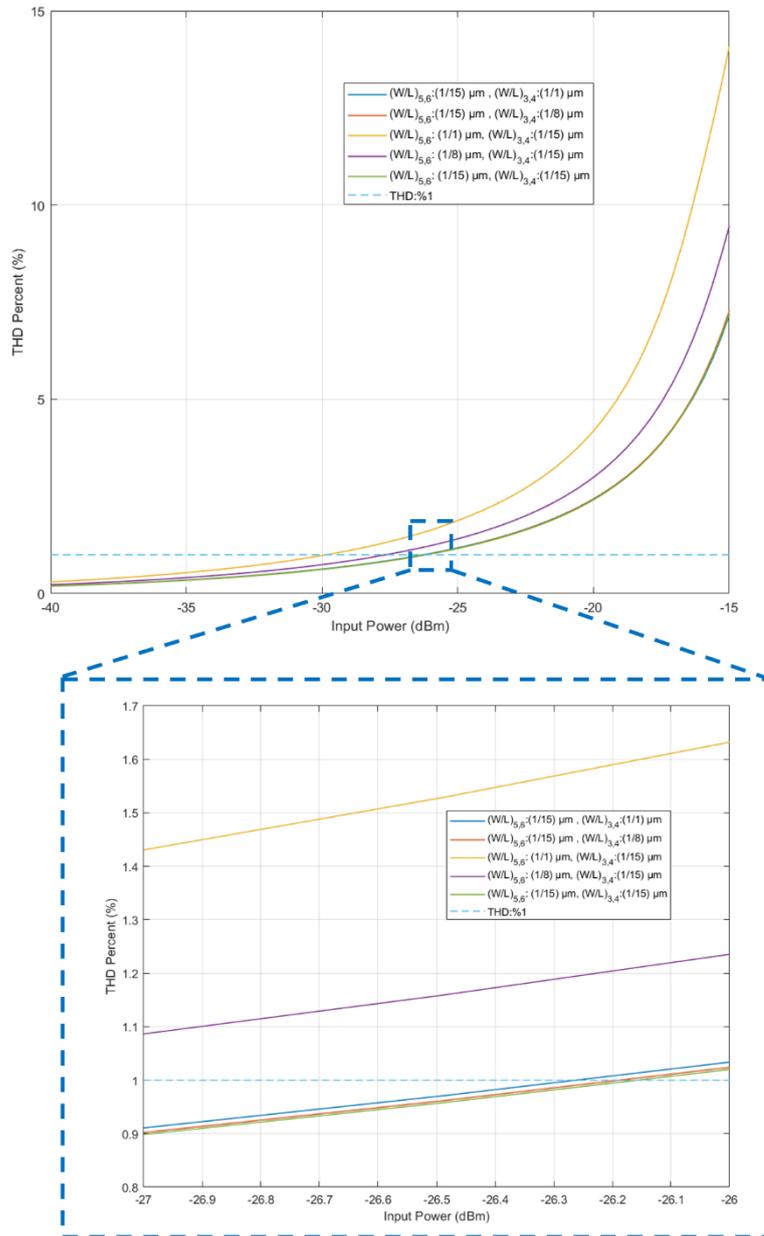


Figure 3.21. The simulated total harmonic distortion of the proposed VGA.

The simulation result is in agreement with the theoretical expectations such that as the aspect ratios of the input pair and degeneration transistors decrease, the linearity of VGA improves. The decrease in the aspect ratio of input pair affects the linearity more compared to the decrease in the aspect ratio of degeneration transistors. Therefore, long channel input transistors are utilized in the design. For the best case, the total harmonic distortion of the proposed VGA remains less than one percent up to the input signal level of 30.98 mV<sub>pp</sub>. However, this results in higher input-referred noise. Figure 3.22 depicts the noise spectral densities of the cases in which the lengths of the input pair are swept as in the simulation of total harmonic distortion. The noise spectral densities are integrated over the target band (85-6500 Hz) and the input-referred noises are calculated as 43.1  $\mu$ V<sub>rms</sub>, 61.6  $\mu$ V<sub>rms</sub>, and 75  $\mu$ V<sub>rms</sub> for the aspect ratios of (1/1)  $\mu$ m, (1/8)  $\mu$ m and (1/15)  $\mu$ m respectively. As these noise levels are reduced by the gains of the previous stages, linearity is preferred over the noise performance in this block to process amplified sensor output effectively.

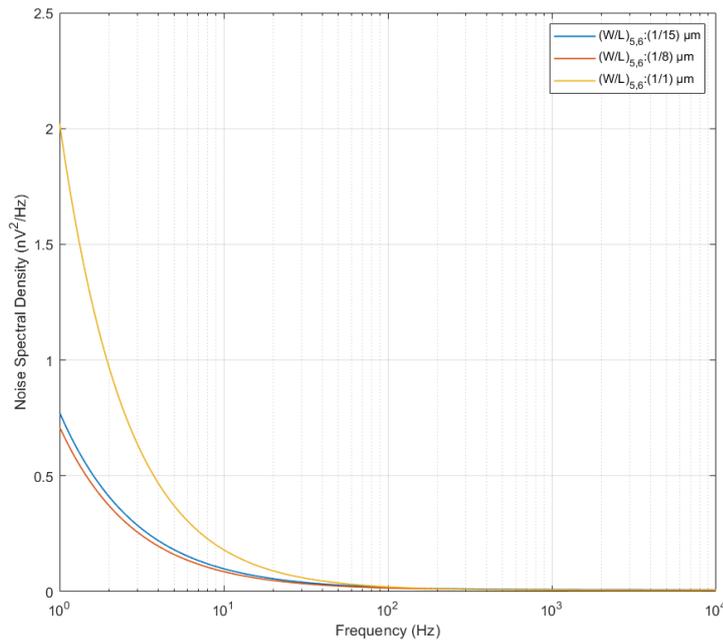


Figure 3.22. The simulated noise spectral densities of VGA for different aspect ratios of input pair.

To program the gain of VGA, the bias current of the second OTA cell is kept constant at 10 nA and the gain is adjusted by varying the bias current of the first OTA cell. Figure 3.23 demonstrates the programmability of the proposed VGA for different bias currents to the first OTA cell. The result also shows that the gain of the proposed VGA is flat throughout the acoustic band thanks to wide bandwidth.

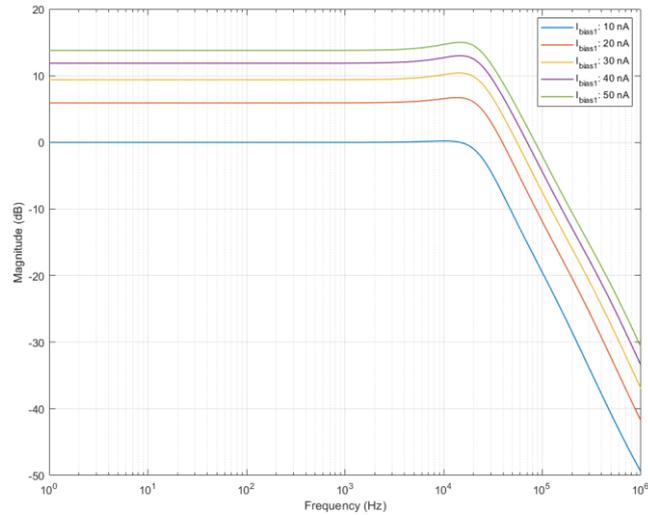


Figure 3.23. The simulated gain programmability of the proposed VGA.

The proposed VGA consumes 143 nW while providing a gain of 9 dB. The power consumption characteristics of the proposed VGA are presented in Figure 3.24.

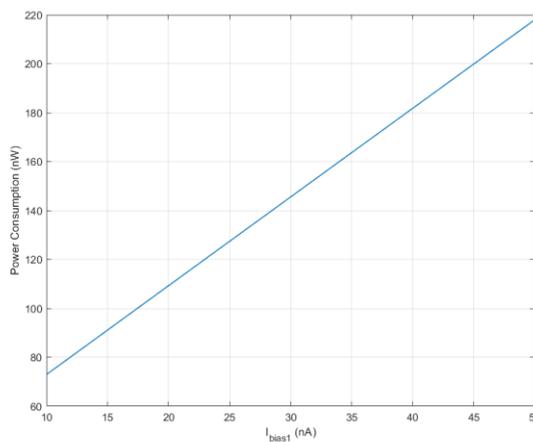


Figure 3.24. The simulated power consumption of the proposed VGA.

The transient response of the proposed VGA is simulated by using the following parameters:  $V_{ref}$ : 500 mV,  $V_{in}$ :  $100 \mu V_{pp}$ ,  $f_{in}$ : 1 kHz,  $I_{bias2}$ : 10 nA,  $I_{bias1}$ : 10-40 nA and high pass filtered output to set DC level 0 V as demonstrated in Figure 3.25. The result shows that the proposed VGA achieves the desired operation as stated in Figure 3.2 while consuming less than 200 nW (12.3 dB gain) and providing improved linearity ( $30.98 mV_{pp}$  @1% THD).

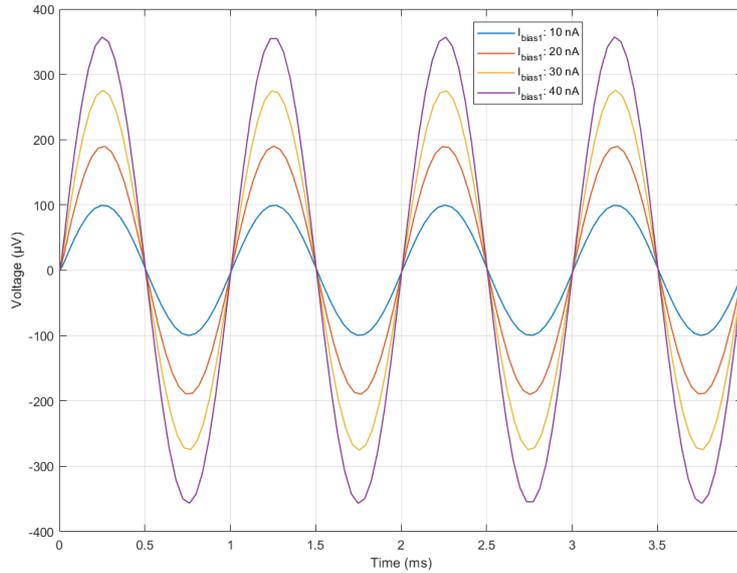


Figure 3.25. The simulated transient response of the proposed VGA.

### 3.3.4 Current Reference

Low power consumption is an important design goal of the proposed analog front-end. To achieve low power operation, most of the transistors in the circuits of LNA, filter bank, and VGAs operate in the subthreshold region so that the operating currents are in the nano ampere range. To make these transistors operate in the subthreshold region stably, supply and temperature-independent DC bias currents in the nano ampere range are required. Thus, a nano ampere current reference that would provide the other blocks with required bias currents is an essential part of the proposed analog front-end.

The beta multiplier (BM) current reference circuit is widely used as it generates a supply insensitive reference current. A simple beta multiplier circuit is depicted in Figure 3.26. In this circuit, an NMOS current mirror with source degeneration through the resistor R is loaded by a PMOS current mirror. The transistors operate in the saturation region and there is a multiplying factor K between the aspect ratios of M3 and M4. To analyze the operation of the circuit, Kirchoff's voltage law (KVL) would be applied through the loop formed by M3, M4, and R as given in the equation (3.17).

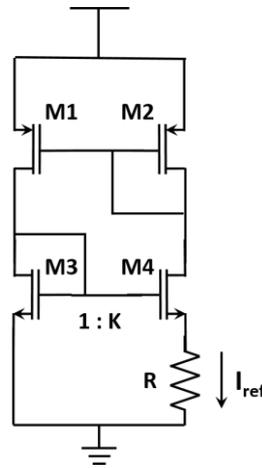


Figure 3.26. The beta multiplier current reference circuit.

$$V_{GS3} = V_{GS4} + I_{ref}R \quad (3.17)$$

The equation (3.17) would be revised by using the saturation current expression as below:

$$V_{th} + \sqrt{\frac{2I_{ref}}{\mu_n C_{ox} \left(\frac{W}{L}\right)}} = V_{th} + \sqrt{\frac{2I_{ref}}{\mu_n C_{ox} K \left(\frac{W}{L}\right)}} + I_{ref}R \quad (3.18)$$

Solving equation (3.18) for  $I_{ref}$  results in:

$$I_{ref} = \frac{2}{R^2 \mu_n C_{ox} \left(\frac{W}{L}\right)} \left(1 - \sqrt{\frac{1}{K}}\right)^2 \quad (3.19)$$

The equation (3.19) indicates that the reference current has no dependency on the supply voltage but the resistor and the sizing of the transistor.

On the other hand, the electron mobility and resistance change with the temperature. The temperature coefficient (TC) of  $I_{ref}$  is calculated by differentiating equation (3.20) with respect to the temperature as given below:

$$TC|_{I_{ref}} = \frac{1}{I_{ref}} \frac{\partial I_{ref}}{\partial T} = -2 \frac{1}{R} \frac{\partial R}{\partial T} - \frac{1}{\mu_n} \frac{\partial \mu_n}{\partial T} \quad (3.20)$$

The dependency of the electron mobility to the temperature would be approximated as  $1.5/T$  [61] which gives a temperature coefficient of 5000 ppm/°C and the typical value for the temperature coefficient of an n-well resistor is around -4000 ppm/°C. Thus the temperature coefficient of beta multiplier current reference is calculated as 1000 ppm/°C [62].

To improve the temperature coefficient of the beta multiplier, the circuit can be modified as illustrated in Figure 3.27 [63]. The transistors of M1-M10 would operate in the subthreshold region to generate current in nano ampere range while M11 operates in the linear region to act as resistance. As in the beta multiplier circuit, KVL would be applied through the loop formed by the transistors of M9-M11 as given in equation (3.21).

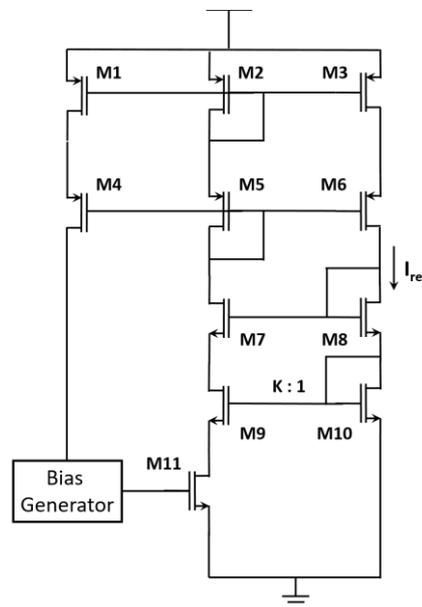


Figure 3.27. The modified beta multiplier current reference [63].

$$V_{GS10} = V_{GS9} + V_{DS11} \quad (3.21)$$

As the currents flowing through the transistors of M9 and M10 are equal, equation (3.21) can be revised as:

$$V_{DS11} = n\varphi_t \ln K \quad (3.22)$$

For a bias voltage  $V_{bias}$  generated by the bias generator block, the reference current is expressed as follows:

$$I_{ref} = \frac{n\varphi_t \ln K}{R} = n\varphi_t \ln K \mu_n C_{ox} \left(\frac{W}{L}\right)_{M11} (V_{bias} - V_{TH}) \quad (3.23)$$

The temperature dependences of the electron mobility and threshold voltage are given as:

$$\mu_n(T) = \mu_n(T_0) \left(\frac{T}{T_0}\right)^{-1.5} \quad (3.24)$$

$$V_{TH}(T) = V_{TH0} - kT \quad (3.25)$$

Where  $V_{T0}$  is the threshold voltage at the temperature of absolute zero,  $k$  is the temperature dependency parameter of the threshold voltage and  $\mu(T_0)$  is the electron mobility at room temperature.

The TC of the reference current can be calculated as follows:

$$TC|_{I_{ref}} = \frac{1}{I_{ref}} \frac{\partial I_{ref}}{\partial T} = \frac{-0.5}{T} + \frac{1}{V_{bias} - V_{TH}} \frac{\partial (V_{bias} - V_{TH})}{\partial T} \quad (3.26)$$

As equation (3.26) indicates, the TC of the reference current can be negative or positive depending on the temperature dependence of the bias voltage [64]. This feature is utilized to generate proportional to absolute temperature (PTAT) current and complementary to absolute temperature (CTAT) current by using different bias blocks so that the summation of these two currents would result in a reference current less sensitive to the changes in the temperature as demonstrated in Figure 3.28. In PTAT block, the transistors of M3 and M4 are implemented as the bias generator which operates in subthreshold and saturation regions respectively. As M13 is implemented to replace the resistor, it operates in the linear region. The difference

between gate-to-source voltages of M4 and M3 sets the bias voltage of M13. Therefore, M4 is a high threshold transistor to generate sufficient bias voltage. In CTAT block, two diode-connected cascode transistors of M16 and M17 are employed as the bias generator and M26 as the resistor. Both of the transistors operate in the subthreshold region and the summation of the gate-to-source voltages of M16 and M17 generates the bias voltage of M26. Different from [63], M17 is a high voltage transistor to provide higher bias voltage. These two currents are mirrored to the third block and summed to generate a reference current which is less sensitive to the temperature variations. This reference current is mirrored to the other blocks with suitable multiplying factors to bias LNA, filterbank, and VGAs.

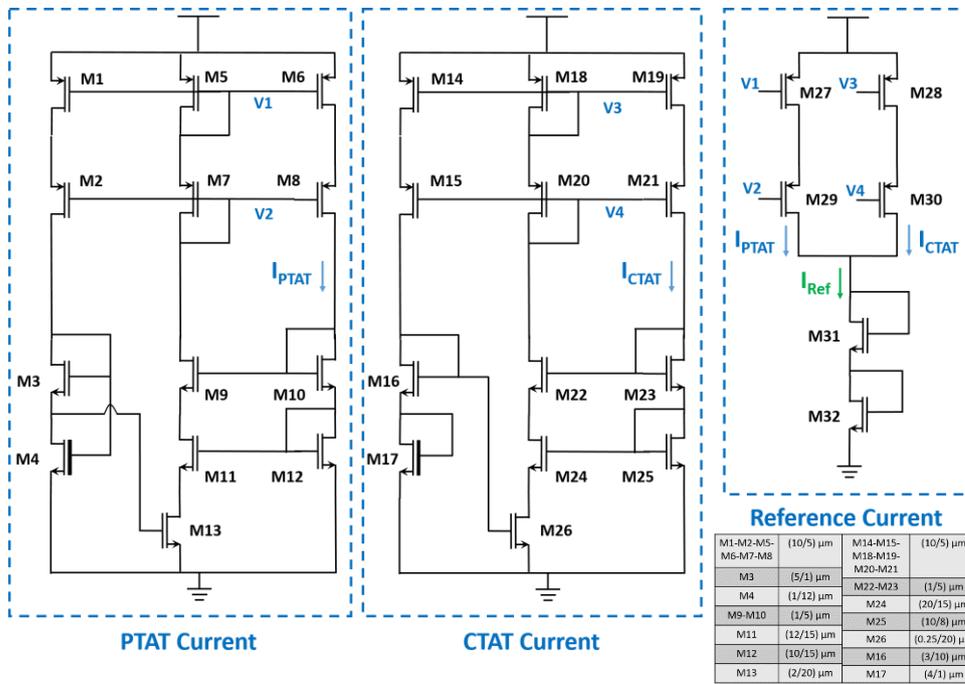


Figure 3.28. The proposed current reference.

The current reference was designed and simulated in TSMC 0.18  $\mu\text{m}$  CMOS technology. The circuit is able to provide a reference current of 28.11 nA under 1.8 V supply voltage and 27  $^{\circ}\text{C}$ . The bias currents of the other blocks would be generated by mirroring this current. Figure 3.29 shows the temperature dependence of the generated currents. The variation in the reference current is observed as 28.11 nA  $\pm 0.7$  nA for the temperature range of 0 to 100  $^{\circ}\text{C}$ .

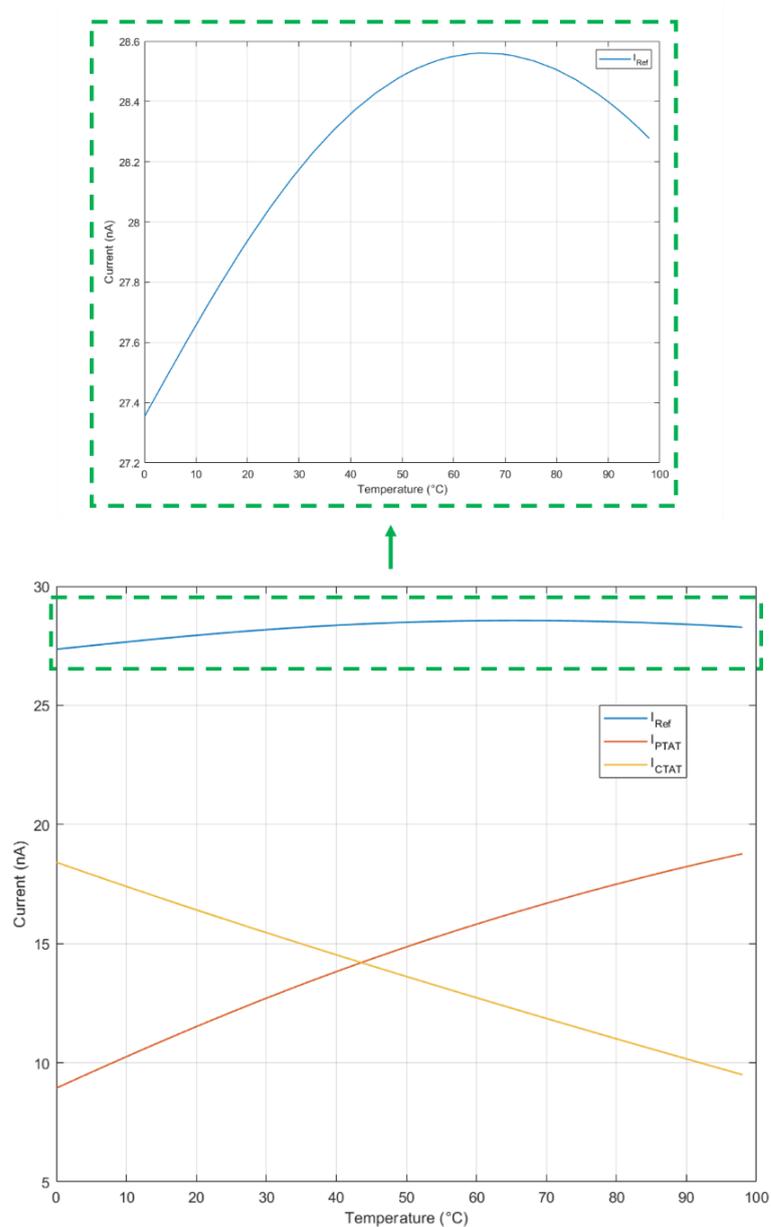


Figure 3.29. The simulated temperature dependence of the proposed current reference.

The supply voltage dependence of the reference current under 27°C is demonstrated in Figure 3.30. The reference current has almost no supply voltage dependence for the supply voltages from 1.2 V to 2.4 V. The variation from 1.6 V to 2V is around  $\Delta I_{Ref}=33$  pA,  $\Delta I_{Ref}/I_{Ref}=\%0.117$  and this is mainly due to the drain induced barrier lowering (DIBL) effect [65].

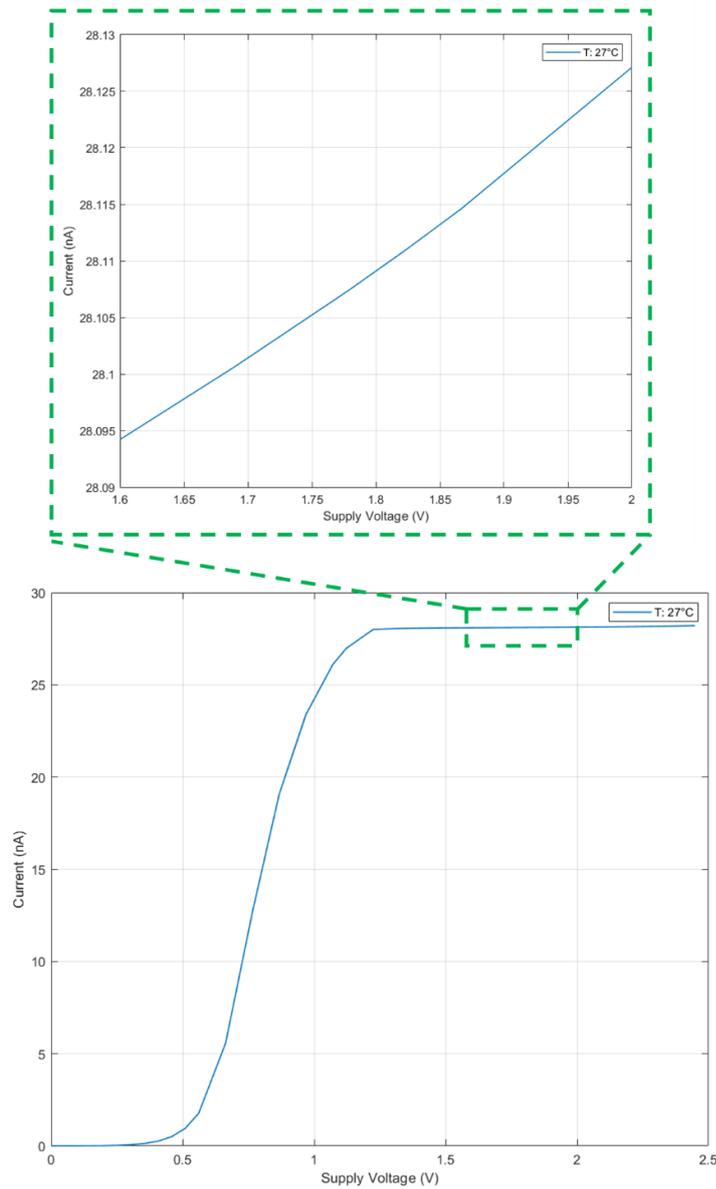


Figure 3.30. The simulated supply voltage dependence of the proposed current reference.

The current reference circuit consumes 255.7 nW under 1.8 V supply voltage and 27°C while providing a reference current of 28.11 nA. Due to the process variations, the reference current would shift from this value. Figure 3.31 demonstrates the Monte Carlo simulation result of the reference current over 200 runs. The result shows that an average reference current of 29.48 nA is obtained with a standard deviation of 9.16 nA.

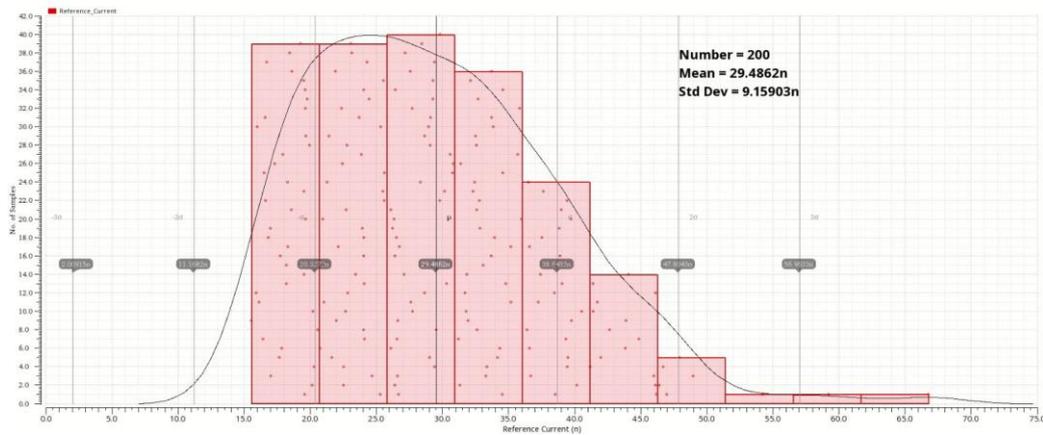


Figure 3.31. The Monte Carlo simulation of the reference current.

### 3.3.5 Control Block

An important feature of the proposed analog front-end is high programmability. There are four programmability options implemented in the design. The first option is the control of LNA bandwidth. The system is designed to interface with a single-channel acoustic sensor mounted onto the ossicles. As the design of a single-channel acoustic sensor is not in the scope of this thesis, the proposed analog front-end should be able to interface with different sensors. In other words, the resonance frequencies of the single-channel acoustic sensors would shift from the desired values to the frequencies within the passband of the LNA after the fabrication. In this case, the bandwidth of the LNA should be reconfigured not to amplify the resonance noise of the sensor. In addition, by tuning the bandwidth of the LNA, the analog front-end would be compatible to interface with any accelerometer-type sensors. The second and third options are related to center frequencies and bandwidths of the filters in the filterbank. To implement best center frequency-bandwidth combinations of the channels for each patient so that the hearing is optimized and recover the lost frequency bands in case of faulty channels, the resonance frequency and bandwidth of each channel can be controlled in this design. Lastly, the signal amplitudes of the channels can be controlled to amplify the magnitudes of specific frequencies before transmitting the signals to the stimulation block.

The design provides four alternatives of LNA bandwidth, four alternatives of center frequency, eight alternatives of bandwidth, and four alternatives of gain. The values of the alternatives for all channels are summarized in Table 3.5. The values in bold represent the default values for the operation of the proposed analog front-end.

Table 3.5 The programmability options and corresponding values

	<i>Ch1</i>	<i>Ch2</i>	<i>Ch3</i>	<i>Ch4</i>	<i>Ch5</i>	<i>Ch6</i>	<i>Ch7</i>	<i>Ch8</i>	<i>Ch9</i>	<i>Ch10</i>	<i>Ch11</i>	<i>Ch12</i>
LNA Bandwidth 1 (Hz)	6651	6651	6651	6651	6651	6651	6651	6651	6651	6651	6651	6651
LNA Bandwidth 2 (Hz)	<b>7545</b>	<b>7545</b>	<b>7545</b>	<b>7545</b>	<b>7545</b>	<b>7545</b>	<b>7545</b>	<b>7545</b>	<b>7545</b>	<b>7545</b>	<b>7545</b>	<b>7545</b>
LNA Bandwidth 3 (Hz)	8434	8434	8434	8434	8434	8434	8434	8434	8434	8434	8434	8434
LNA Bandwidth 4 (Hz)	9317	9317	9317	9317	9317	9317	9317	9317	9317	9317	9317	9317
Filter Center Frequency 1 (Hz)	85	162	269	407	575	812	1000	1348	1820	2454	3311	4466
Filter Center Frequency 2 (Hz)	<b>125</b>	<b>218</b>	<b>331</b>	<b>489</b>	<b>691</b>	<b>954</b>	1101	1513	2041	2754	3630	4898
Filter Center Frequency 3 (Hz)	166	269	407	575	812	1100	<b>1318</b>	<b>1778</b>	<b>2350</b>	<b>3236</b>	<b>4265</b>	<b>5754</b>
Filter Center Frequency 4 (Hz)	186	295	436	631	891	1201	1513	2041	2754	3630	4898	6606
Filter Bandwidth 1 (Hz)	33	64	71	115	171	213	292	421	558	739	838	1246
Filter Bandwidth 2 (Hz)	49	79	88	135	193	239	324	454	597	798	945	1351
Filter Bandwidth 3 (Hz)	65	94	105	154	215	265	357	485	639	858	1054	1453
Filter Bandwidth 4 (Hz)	<b>80</b>	<b>109</b>	<b>122</b>	<b>173</b>	<b>237</b>	<b>291</b>	<b>389</b>	<b>517</b>	<b>680</b>	<b>917</b>	<b>1161</b>	<b>1557</b>
Filter Bandwidth 5 (Hz)	96	124	139	192	259	317	421	548	720	976	1268	1659
Filter Bandwidth 6 (Hz)	111	139	155	211	280	343	453	578	762	1036	1374	1760
Filter Bandwidth 7 (Hz)	127	154	172	229	302	369	485	610	802	1093	1479	1862
Filter Bandwidth 8 (Hz)	142	168	189	248	323	394	516	640	842	1152	1584	1963
VGA Gain 1 (dB)	0	0	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
VGA Gain 2 (dB)	<b>4.4</b>	<b>4.4</b>	4.4	4.4	4.4	4.4	4.4	4.4	4.4	4.4	4.4	4.4
VGA Gain 3 (dB)	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5
VGA Gain 4 (dB)	12.4	12.4	12.4	12.4	12.4	12.4	12.4	12.4	12.4	12.4	12.4	12.4

As all blocks in the design are biased by the currents, the programmability is achieved by controlling the bias currents to the blocks. Thus, a control block is designed to regulate the control of the system digitally as shown in Figure 3.32.

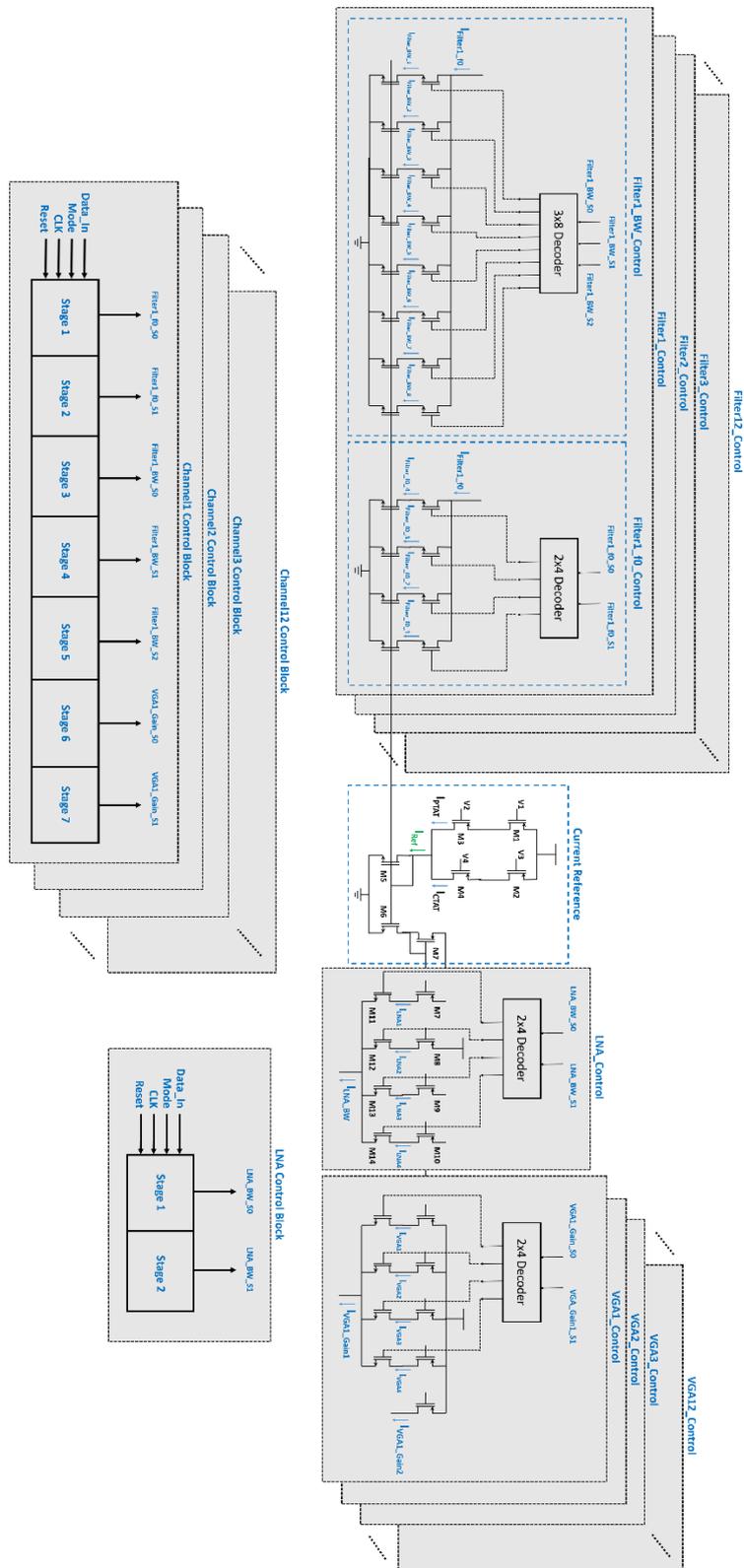


Figure 3.32. The control block of the proposed analog front-end.

The operational principle of the control block is based on the digital control of the reference current mirroring. Each block includes a set of mirroring transistors. The number of these transistors are related to the programmability options of the corresponding block (i.e. LNA: 4, filterbank: 12x(4+8), VGAs: 12x4). Each mirroring transistor has a specific multiplying factor to generate the corresponding bias current for the desired programmability option from the reference current. The flows of the generated currents are digitally controlled by the decoders. The digital bits of the decoders decide which current would bias the block. Therefore, there are two bits to control the bandwidth of the LNA, two bits for the center frequency of the filter, three bits for the bandwidth of the filter and two bits for the gain of the VGA. To sum up, there are two common bits for LNA and 7 bits for the filter and VGA of each channel. Considering 12 channel operation, 86 bits are required to have full control on the proposed analog front-end. Therefore, the inputs to the control pins should be applied serially and loaded to the blocks in parallel. To realize this operation, universal shift registers are implemented. These shift registers would get input data serially and shift the bits in each clock. When the desired pattern is loaded, the control pins of the shift registers are set such that the shift registers hold the loaded data. A sample loading of a serial input to the channel 1 control block is illustrated in Figure 3.33. The control block accepts inputs only when  $S_1S_0$ : 01.

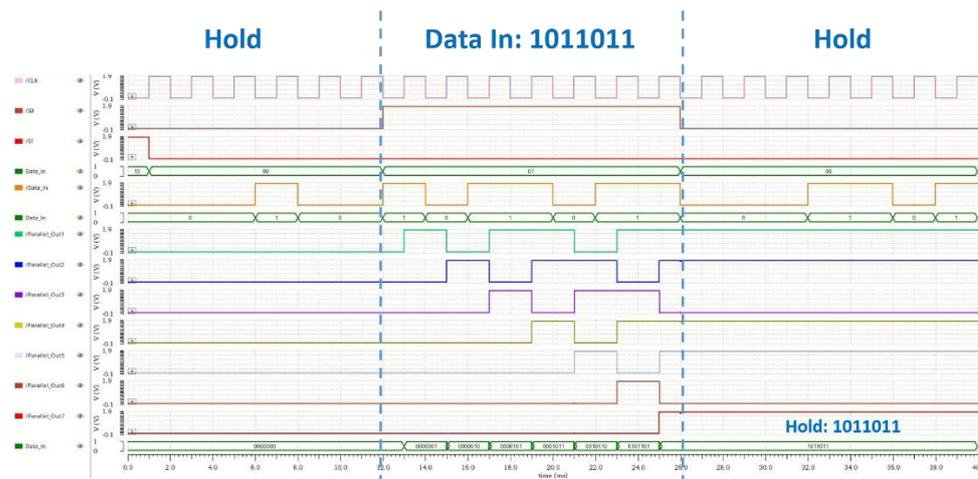


Figure 3.33. The loading of the serial input “1011011” by the control block.

Referring to table Table 3.5, this input sets the center frequency of the first filter to 166 Hz as the first two bits are “10” which corresponds to the third alternative of the center frequency. The following three bits “110” set the bandwidth of the first filter to 111 Hz. The last two bits of “11” adjust the gain of the first VGA as 12.4 dB.

### 3.4 Simulation Results

The proposed analog front-end was designed and simulated in TSMC 0.18  $\mu\text{m}$  CMOS High Voltage BCD process. The chip occupies an active area of 2.4  $\text{mm}^2$  as shown in Figure 3.34. The desired operation of the proposed analog front-end is demonstrated in Figure 3.2. The functionality of the blocks in the design and the overall operation are successfully verified through simulation results.

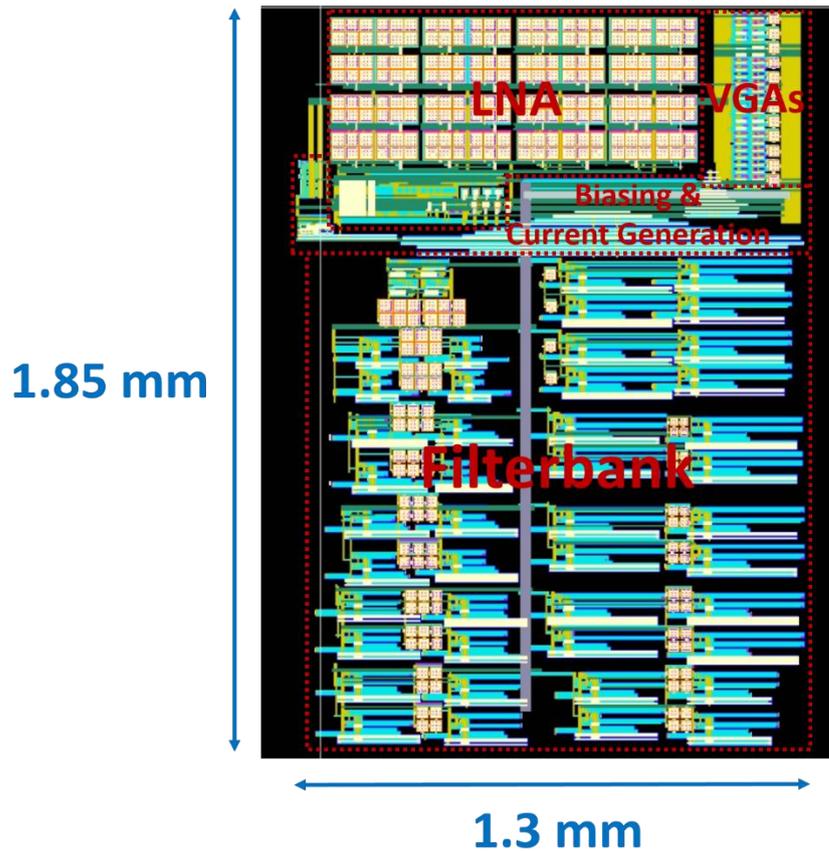


Figure 3.34. The layout of the proposed analog front-end circuit.

### 3.4.1 Single-Tone Signal Flow

The flow of the input signal is explained through channel 6. As a sample single-tone input signal, a sinusoidal wave with a frequency of 954 Hz (center frequency of 6<sup>th</sup> channel) and amplitude of  $20 \mu\text{V}_{\text{pp}}$  is applied to mimic the output of the acoustic sensor. The first block of the analog front-end, LNA, amplifies the input signal to the millivolt range with very low input-referred noise as shown in Figure 3.35.

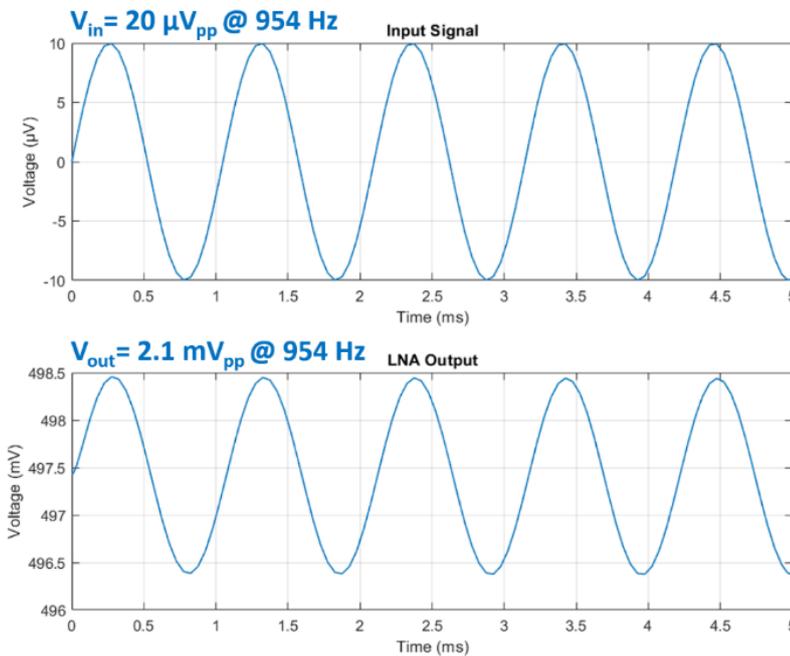


Figure 3.35. The signal flow through the LNA.

The LNA amplifies the amplitude of the input signal from  $20 \mu\text{V}_{\text{pp}}$  to  $2.1 \text{mV}_{\text{pp}}$  which corresponds to a gain of 40.4 dB. Since the filters would amplify the signal in passband as well, the gain of the LNA is lowered slightly from the mentioned value of 44.3 dB. In addition, the DC level of the signal is shifted from 0 to 500 mV through the common-mode feedback of the LNA in order to keep the bulk-source diodes of the filters closed. Although there is a small DC offset, this does not affect much the operations of the filters except a small gain variation which would be compensated by the VGAs. The output of the LNA is processed by the filterbank as illustrated in Figure 3.36.

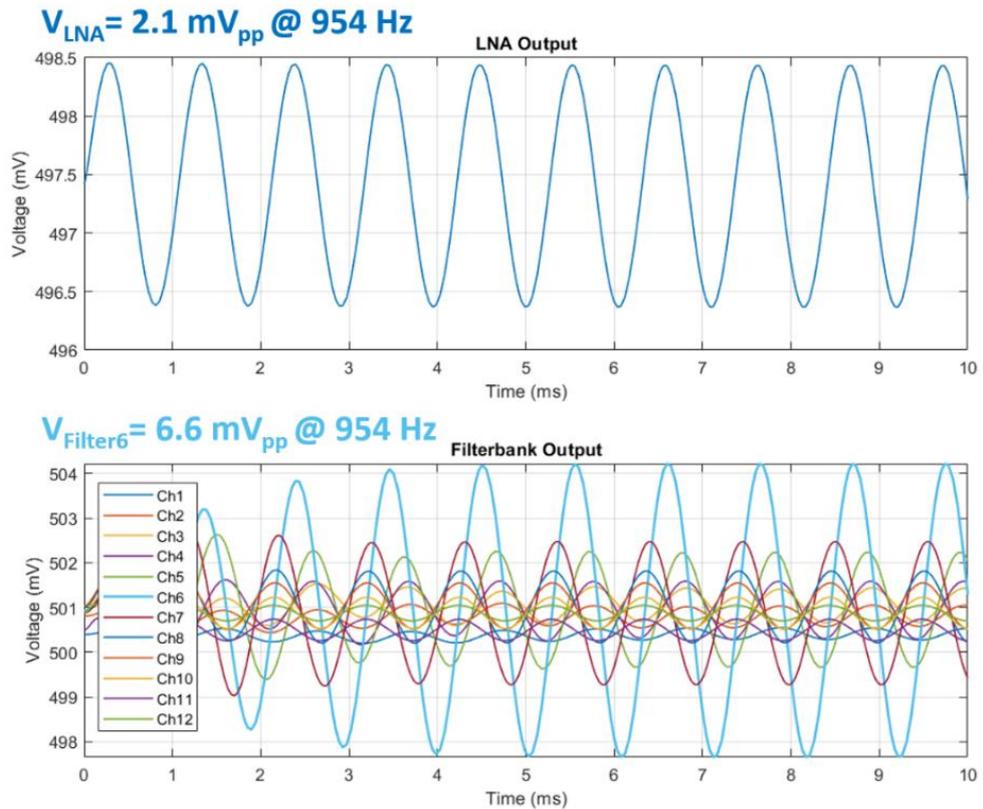


Figure 3.36. The signal flow through the 6<sup>th</sup> filter.

Each filter in the filterbank preserves (or small amplification) the signal with channel frequency while suppressing the signals whose frequencies are other than the channel frequency depending on the quality factor of the channel. In the sample case, the frequency of input signal is the same as the channel 6 frequency. Therefore, the filter in channel 6 passes the output of LNA with a small amplification of 9.9 dB while the filters of other channels provide a suppressed output. The suppressions of the filters depend on the proximity of the frequency of the related channel to channel 6.

After decomposing the input signal into the frequency components in the filter bank, the outputs of the filters are fed to the VGAs to set the final amplitude of the signal before transmitting to the stimulation block of the fully implantable cochlear implant. As the input signal should flow through channel 6 in the sample case, the operation of the sixth VGA is demonstrated in Figure 3.37.

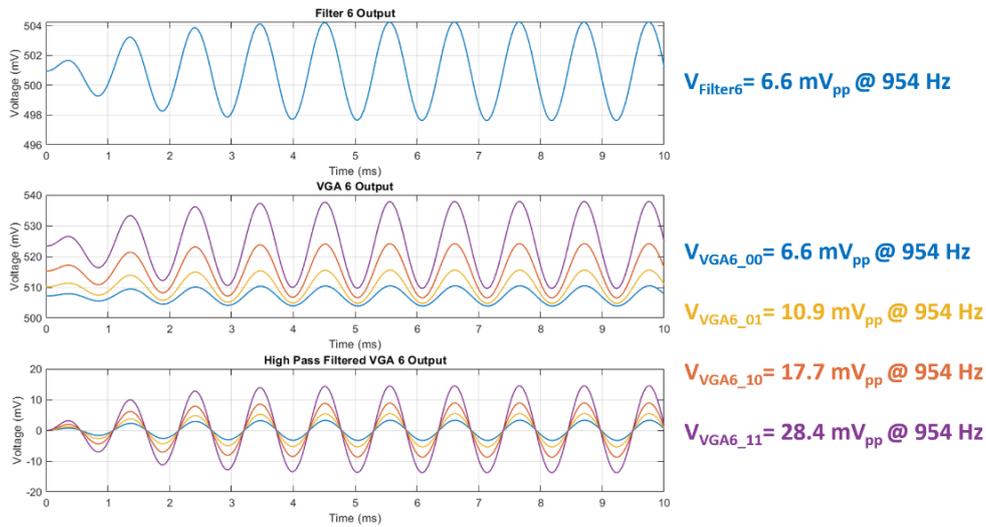


Figure 3.37. The signal flow through the 6<sup>th</sup> VGA.

The VGA of channel 6 is able to amplify the output of filter 6 based on the gains given in Table 3.5. The control of the gain is realized by loading proper inputs to the control block. The drawback of the block is that the VGAs introduce DC offsets depending on the gains. If the first block of the stimulation part can work under the DC level of 500 mV with  $\pm 25$  mV for this case, the offset would not be a problem. As a solution, the signal would be filtered by a high pass filter to set the DC level as 0 V as depicted in Figure 3.37.

The sample case shows that the desired operation indicated in Figure 3.2 is achieved by the proposed analog front-end. All channels process pure tone inputs whose frequencies are the same as the frequencies of the corresponding channels as explained in the channel 6 case.

### 3.4.2 Multi-Tone Signal Flow

The sounds are composed of many tones with different amplitudes, frequencies, and phases. Therefore, to model the real sound, the input signal applied to the proposed analog front-end should contain multi-tone signals. The system should decompose this input into the frequency components such that the dominant frequency at the

output of each channel should be the frequency of that channel. However, the cochlea senses any frequency in the acoustic band continuously while the cochlear implants sense the frequencies discretely depending on the electrode number. In other words, for the 12-channel case, the cochlear implant should cover any frequency in the acoustic band with 12 discrete center frequencies. To achieve this, the channels should contain information of the frequencies close to the channel frequencies as well. Therefore, it is not expected to observe a single tone frequency at the outputs of the channels. This characteristic is observed through two simulations.

In the first case, the input signal contains 2 tones whose frequencies are the center frequencies of channel 6 and 12 with the same magnitude as demonstrated in Figure 3.38. Since the input signal has no frequency components of other channels, the dominant frequency of these channels is the frequency of the closest channel. In other words, 954 Hz is dominant in channels 1-6. After that, the effect of 5754 Hz becomes visible and this frequency becomes dominant after channel 9.

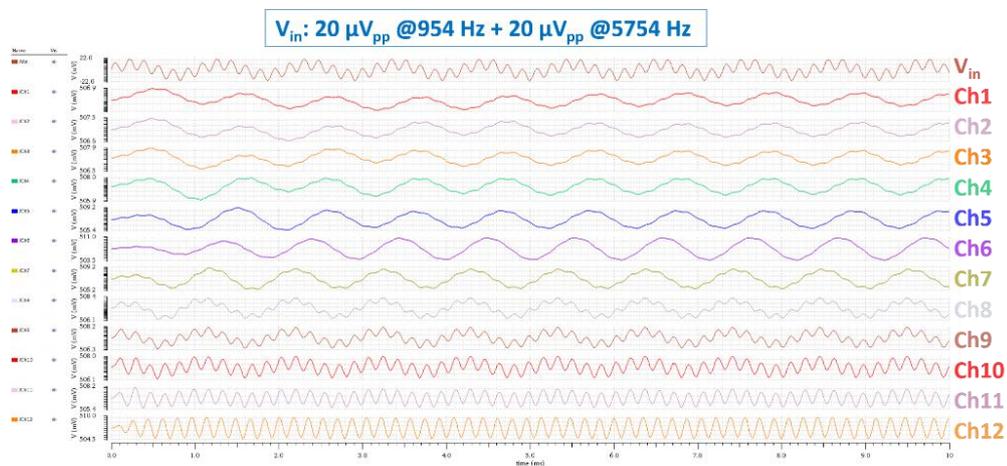


Figure 3.38. The response of the analog front-end to the input with 2 tones.

The second case introduces an input with 9 tones whose frequencies are the center frequencies of the channels 1-9 with the same amplitude as illustrated in Figure 3.39. As the input signal has frequency components of channel 1-9, the dominant frequencies are the channel frequencies. As the input signal has no frequency components of the channels 10-12, these channels suppress the input signal and have a dominant frequency of the closest channel (2350 Hz).

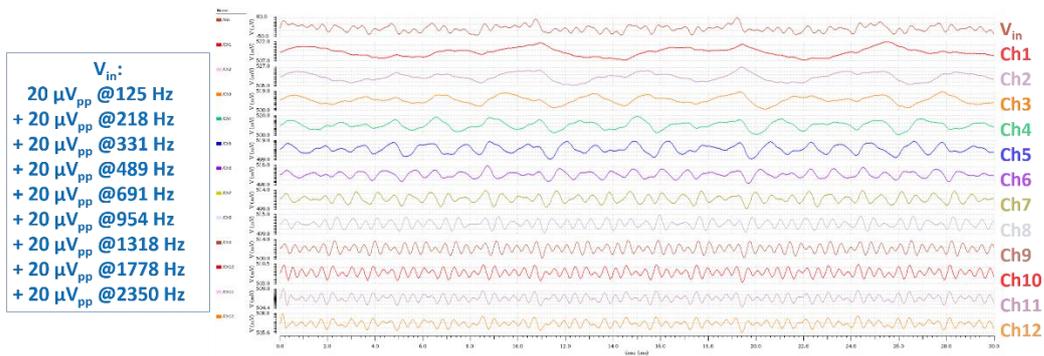


Figure 3.39. The response of the analog front-end to the input with 9 tones.

These two results indicate that there are no pure tone signals at the outputs of the analog front-end and each channel contains information of the frequencies close to the channel as expected. This characteristic would provide the cochlear implant with stimulation of the frequencies which do not have a specific node in the electrode as desired. The results are compatible with the responses of the filterbanks in conventional cochlear implants [66].

### 3.4.3 Digital Control of the Blocks

The parameters that can be controlled in the proposed analog front-end are the bandwidth of the LNA, the center frequencies and bandwidths of the filters in the filter bank and, the gains of the VGAs. These parameters are controlled digitally from the outside by using the control block of the system. The alternatives for these parameters are summarized in Table 3.5. By loading the desired inputs serially as illustrated in Figure 3.33, the parameters are controlled based on the values indicated in Table 3.5 as shown in Figure 3.40, Figure 3.41, Figure 3.42 and, Figure 3.43. Thanks to this block, an audiologist can easily adjust the system parameters through a computer software based on the feedbacks of the patients so that the speech perception would be maximized for each patient.

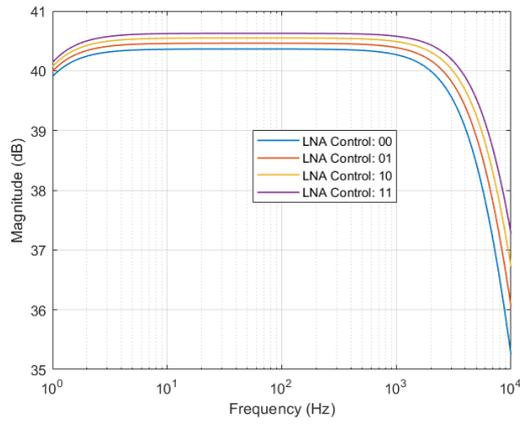


Figure 3.40. The bandwidth control of LNA.

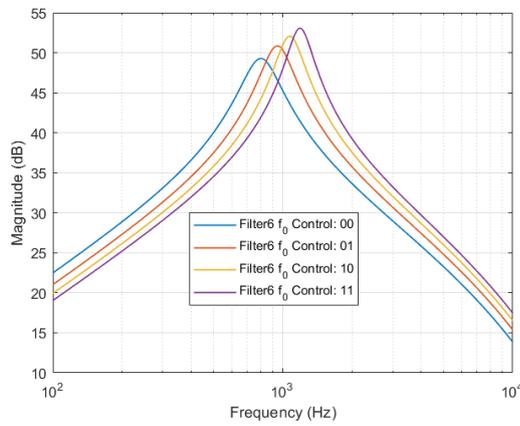


Figure 3.41. The center frequency control of channel 6.

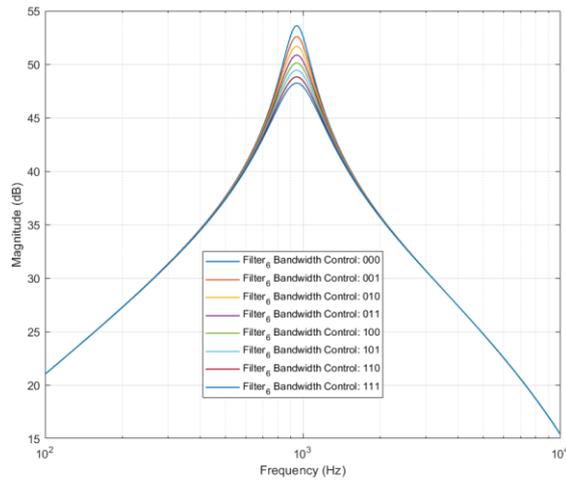


Figure 3.42. The bandwidth control of channel 6.

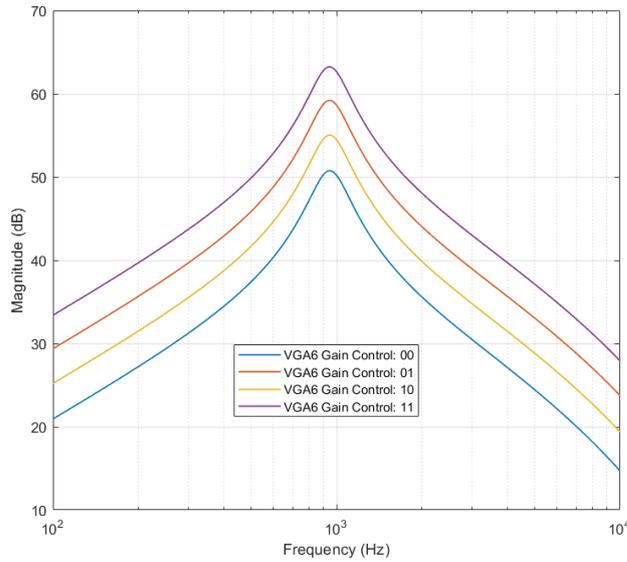


Figure 3.43. The gain control of channel 6.

### 3.4.4 Lost Band Recovery

There might be an incomplete insertion of the electrodes to the cochlea during the operative procedure. The incomplete nodes cause a reduction in the hearing of corresponding frequency bands. Moreover, the impedances of the nodes would increase over time and this degrades the performance of the related channel. The revision of the problematic nodes would be a solution but it is an invasive method. Therefore, controlling the center frequencies and bandwidths of the remaining channels would provide a non-invasive solution. By rearranging the frequency and bandwidth distributions of the remaining channels, the lost band would be recovered.

The proposed analog front-end is able to recover the lost bands in case of faulty or incomplete channels. Figure 3.44 shows a sample case such that channels 2 and 10 are lost due to the mentioned reasons. To recover the lost bands of channel 2, the center frequency of channel 3 is shifted to its first alternative (towards channel 2) and the bandwidth is adjusted to its sixth alternative (widen). To recover the lost bands of channel 10, the center frequency of channel 9 is shifted to its fourth

alternative (towards channel 9) and the bandwidth is tuned to its sixth alternative (widen). Thus, the acoustic band is covered by the remaining 10 channels successfully and the loss in hearing is recovered.

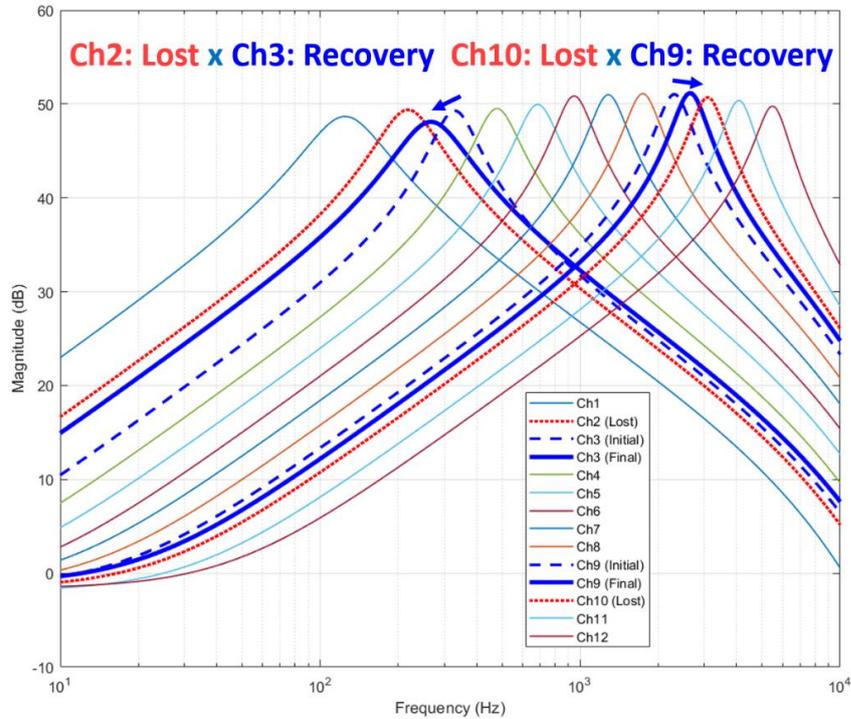


Figure 3.44. The lost band recovery of the proposed analog front-end.

### 3.4.5 Noise and Power

To process outputs of the acoustic sensor in microvolts range, the noise levels of the channels should be low enough so that the hearing threshold is lowered. The input-referred noise levels of the channels which are calculated by integrating the noise spectral densities over the channel bandwidths are kept lower than  $5 \mu\text{V}_{\text{rms}}$  as given in Table 3.6. Thus, for an acoustic sensor whose sensitivity is around  $20 \text{ mV}_{\text{rms}}/\text{g}$ , the proposed analog front-end is able to achieve a hearing threshold of 35 dB for high-frequency signals ( $< 5 \text{ kHz}$ ) (interpolated from [21]) and 60 dB for low-frequency signals ( $< 500 \text{ Hz}$ ) with signal-to-noise ratios of 12.6-21 dB (depending on the channel noise).

Table 3.6 The input-referred noises of the channels

	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12
Input-referred Noise ( $\mu\text{V}_{\text{rms}}$ )	1.78	1.57	1.56	1.58	1.75	1.85	2.13	2.31	2.67	3.21	4.29	4.67

While achieving these hearing thresholds and providing high programmability, the power consumption of the system should be low enough to extend the battery life of the cochlear implant. The proposed analog front-end consumes  $9.03 \mu\text{W}$  with default parameters. The worst-case (highest bias current for each parameter) power consumption is observed as  $14.34 \mu\text{W}$  and the best case (lowest bias current for each parameter) power consumption as  $7.84 \mu\text{W}$ .

The possible shifts from the intended operation due to the process variations are demonstrated through the Monte Carlo simulation for the center frequency of channel 6 in Figure 3.45. The result shows that a mean center frequency of 970 Hz with a standard deviation of 173 Hz is obtained while the intended center frequency is 954 Hz. This shift would be compensated by using the frequency alternatives of the channels. There are four alternatives for the center frequency of channel 6 which are 812, 954, 1100, and 1201 Hz. The standard deviation from the mean value lies in between these alternatives such that a shift from 970 Hz to 800 Hz would be compensated by adjusting the center frequency of channel 6 to 812 Hz.

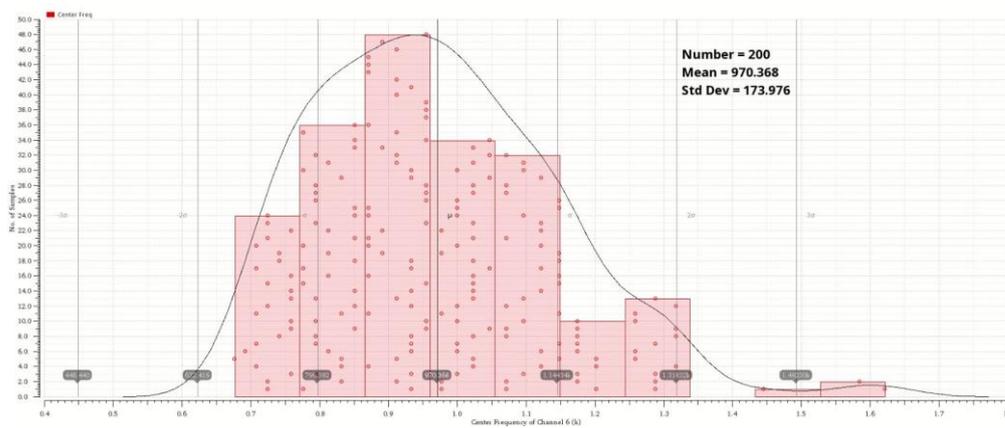


Figure 3.45. The Monte Carlo simulation for the center frequency of channel 6.

### 3.5 Summary and Discussion

The proposed analog front-end is designed to interface with an acoustic sensor mounted onto the ossicles so that the combination of the acoustic sensor and proposed analog front-end would result in a novel fully implantable cochlear implant system. Due to the coupling loss and non-resonance mode operation, the output of the acoustic sensor is predicted to be in the microvolts range depending on the input sound pressure level and frequency. The analog front-end is expected to interface with the acoustic sensor successfully such that the low-level outputs of the sensor are amplified and decomposed into the frequency components. While realizing these operations, the analog front-end should consume low power to extend the battery life of the implant and provide controllability of system parameters to achieve the best speech perception for each individual.

Table 3.7 Performance summary of the blocks in the analog front-end

	<i>Supply</i>	<i>Gain</i>	<i>Low-frequency Cut-off</i>	<i>High-frequency Cut-off</i>	<i>Integrated Noise</i>	<i>Linearity</i>	<i>Power Consumption</i>
LNA	1.8 V	40.4 dB	0.5 Hz	6.6-9.3 kHz (2 bits)	6.14 $\mu V_{rms}$ (85-6500 Hz)	THD 1% @ 1.92 mV <sub>pp</sub>	2.34 $\mu W$
Filterbank	1 V	4.3-11.4 dB	12-channel (2+3) bits	12-channel (2+3) bits	159.3-309.1 $\mu V_m$ (Passband)	1 dB Comp. @ 1.89 mV <sub>pp</sub>	58.1-402 nW
VGAs	1.8 V	0-12.3 dB (2 bits)	-	26.5-33.1 kHz	75 $\mu V_m$ (85-6500 Hz) @ 9 dB	THD 1% @ 30.98 mV <sub>pp</sub>	143 nW @ 9 dB

The simulation results verify that the proposed analog front-end meets these expectations as summarized in Table 3.7. The outputs of the acoustic sensor greater than 20  $\mu V_{rms}$  are amplified to the millivolts range with an SNR of at least 12.4 dB. The amplified output is processed by the filterbank such that the signal is decomposed into the frequency components by 12 channels based on the best center frequency-bandwidth combinations. Each frequency component can further be amplified by the VGAs before transmitting to the stimulation block.

Besides these operations, the bandwidth of the LNA would be controlled between 6.6-9.3 kHz to make the system compatible with acoustic sensors which have different resonance frequencies, the center frequencies and bandwidths of the channels in the filter bank would be programmed to achieve the best speech perception and recover the lost bands in case of faulty channels and the gains of each frequency would be adjusted to amplify (0-12.3 dB) specific frequencies. During all these operations, the proposed analog front-end with default system parameters consumes only 9.03  $\mu\text{W}$  (~1.3% of overall power consumption of 12-channel FICI system [26]).

The performance summary indicates that the system is able to accomplish the design specifications such that the power consumption (9.03  $\mu\text{W}$ ) is lower than the limitation of 10  $\mu\text{W}$ , the input-referred noises (worst channel: 4.67  $\mu\text{V}_{\text{rms}}$ ) are better than the limitation of 20  $\mu\text{V}_{\text{rms}}$  and the system is highly programmable. However, for inputs with high SPL, the linearity of the system is not sufficient which the drawback of the design is. In such cases, 40.4 dB amplification of the acoustic sensor exceeds the linear range of the filterbank due to poor linearity performance of the filters which is caused by the reduced transconductances of OTAs. The solution would be reducing the LNA gain such that the amplified outputs of the acoustic transducer stay between the input-referred noises of the filters and signal levels where THDs of the filters are less than 1%. The reduction in the LNA gain would be compensated by increasing the gains of the filters (as VGAs have a better linearity performance) or VGAs (depending on the linearity of the following channel in the stimulation part).

## CHAPTER 4

### CONCLUSIONS AND FUTURE WORK

In this thesis, a low noise, low power, and highly programable analog front-end that interfaces with an implantable acoustic sensor for 12-channel fully implantable cochlear implants has been designed. The system is able to process very low-level outputs of the acoustic sensor so that the incoming sound is sensed, amplified, and decomposed into the frequency components. The proposed analog front-end covers the acoustic band of 85-6500 Hz with 12 channels each of which has a specific bandwidth to provide a near-natural hearing. The center frequencies and bandwidths of the channels can be reconfigured after the implantation so that the hearing would be optimized for each individual and the lost bands of faulty channels due to incomplete insertion or impedance change would be recovered. While all channels are actively operating, the system consumes only 9.03  $\mu$ W. The operation of the filters is observed through experiments and the overall system through simulations. The results validated the concept and demonstrated successful acoustic signal processing of the system so that the proposed analog front-end would be a promising candidate for the speech processing of next-generation fully implantable cochlear implants with acoustic sensors.

#### 4.1 Summary of Contributions

The outcomes of the research in this thesis can be summarized as follows:

1. A highly tunable second-order  $G_m$ -C bandpass filter formed by bulk-driven subthreshold folded cascode OTAs has been designed and implemented in TSMC 0.18  $\mu$ m CMOS High Voltage BCD process. Bulk driving technique combined with subthreshold operation helps the filter to cover low frequencies of the acoustic band (<1 kHz). The control of the

transconductances through bias currents in  $G_m$ -C topology provides the filter with high tunability on the center frequency and bandwidth of the filter. The experimental results demonstrated that the filter is able to cover the acoustic band of 100-8000 Hz with a tunable quality factor, achieves a dynamic range of 51.98 dB, and consumes only 13.2 nW at 950 Hz under 1 V supply. Thus, the filter achieves one of the best FoMs compared to the analog bandpass filters reported in the literature and the filter would be considered as an ideal candidate for the auditory signal processing of fully implantable cochlear implants.

2. A supply and temperature insensitive current reference has been designed in the same process to generate bias currents of the blocks so that autonomous operation is achieved. The circuit generates PTAT and CTAT currents and the summation of these currents results in a reference current of 28.11 nA which varies  $\pm 0.7$  nA for the temperature range from 0 to 100°C. The circuit operates under a 1.8 V supply and a normalized variation of  $\Delta I_{Ref}/I_{Ref} = 0.117\%$  is achieved from 1.6 V to 2 V while consuming 255.7 nW.
3. An LNA has been designed in the same process to improve the minimum signal level of the filters so that the hearing threshold would be lowered. The orthogonal current reuse structure with 2 Tohms pseudo-resistors achieves an input-referred noise of 6.14  $\mu V_{rms}$  (85-6500 Hz), 40 dB gain, programmable bandwidth of 6.6-9.3 kHz and 2.34  $\mu W$  power consumption. The common-mode feedback of the amplifier sets the output DC level convenient such that the junction diodes of the filters are closed.
4. A VGA has been designed in the same process to control the final amplitudes of the signals in the channels before transmitting to the stimulation part. The circuit achieves a THD less than 1% up to 30.98 mV<sub>pp</sub>, a programmable gain of 0-12.3 dB, and power consumption less than 200 nW at 12.3 dB gain. The

VGAs in the channels are able to equalize the signal magnitudes of the channels or amplify specific frequencies by controlling from the outside.

5. A low noise, low power, and highly programmable analog front-end including LNA, filterbank, and VGAs has been designed in TSMC 0.18  $\mu\text{m}$  CMOS High Voltage BCD process to interface with an implantable acoustic sensor of a FICI. The system is able to successfully process low-level outputs of the sensor ( $>20 \mu\text{V}_{\text{rms}}$ ) as in the speech processors of conventional cochlear implants and mimics the operation of the cochlea with 12 channels (85-6500 Hz) while consuming only 9.03  $\mu\text{W}$  which is one of the lowest power consumption among the analog front-ends for the cochlear implants to the best of my knowledge. Even though the processing is realized in the analog domain, it is possible to reconfigure the parameters of the analog front-end such that the system becomes compatible with different acoustic sensors and maximizes the hearing for each patient. The simulation results demonstrated that the lost frequency bands due to impedance change or unsuccessful insertion of the cochlear electrode can be recovered after the implantation by rearranging the center frequencies and bandwidths of the remaining channels through the digital control of the system.

## **4.2 Future Work**

The research in this thesis can be further improved as indicated in following items:

1. Although the operation of the analog front-end is validated through simulation results, the system should be implemented and the operation of the analog front-end should be observed experimentally. The variations from the simulation results should be extracted and the design should be revised accordingly. In addition, the digital control block of the system should be combined with the wireless data transfer block and the calibration procedure should be developed.

2. The hearing threshold of the analog front-end is 35 dB for high-frequency signals and 60 dB for low-frequency signals. Considering a conversation in a restaurant corresponds to 60 dB, the processing of low-frequency signals is not sufficient for an ideal hearing. Therefore, the minimum signal level which analog front-end can process should be further lowered.
3. The system can handle low-level outputs of the acoustic sensor. However, the patients might be exposed to high-level sounds. In such cases, the output of the acoustic sensor is higher. Considering the amplification of these signals by the LNA, the linear ranges of the filters would not be sufficient due to reduced transconductances. Therefore, the maximum signal level that the analog front-end can process without significant distortions should be improved.
4. The analog front-end should be combined with an acoustic sensor mounted onto the ossicles and stimulation block to achieve a fully implantable cochlear implant system. The operation of these blocks working together should be observed. In case of success, it is proven that the combination of these blocks would result in a novel fully implantable cochlear implant system.

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